Analog and Telecommunication Electronics

C7 - PLL digital applications
  » PSK demodulation
  » Clock resynchronization
  » Clock/data recovery (CDR)

AY 2015-16
Lesson C7: PLL digital applications

- Clock synchronization
  - Clock multipliers
  - Resynchronization with DLL

- Clock-data recovery (CDR)
  - Self-synchronizing serial transmission and embedded clock

- PSK demodulator
  - Lock of phase-modulated signals

- References:
  - D. Del Corso: Elettronica per Telecomunicazioni:
    Synchronizers and clock/data recovery sect. 3.7.3
    Clock multiplier and resynchronizers sect. 3.7.6
High speed digital systems

- Problems for distribution of fast clocks
  - Clock signal reaches various areas with different delays
  - Data from various areas exhibit skew
  - Possibility of synchronization errors (metastability)

- Limited extension of synchronous areas
  - Local fast clock (chip level)
  - Slower global clock (Board)

- How to keep various areas synchronized?
  - Single global clock
  - Local frequency multiplication
  - Local resynchronization
Clock multipliers

- Unique timing reference for various ICs
- Complex systems need clocks at various frequencies, with
  - Known phase relation
  - Time margins for data setup and hold
- PLL clock multipliers
  - Integer synthesizers
  - On-chip clock frequency change capability
    » Performance and power consumption control
  - Fast clocks confined within single ICs
Clock multiplier

- PLL Synthesizer: \( F_{CKI} = N \times F_{CKE} \)

\[ \text{External Clock (} F_{CKE} \text{)} \]

\[ \text{DF} \quad F \quad \text{VCO} \]

\[ R \times N \]

\[ \text{Clock to internal registers (} F_{CKI} \text{)} \]

\[ \text{Clock to interface registers} \]
Clock skew

- The different delays of clock distribution trees causes significant skew between output data.
Effects of clock skew

- Due to skew, output data become valid at different times
- The delay skew limits the clock rate (min. clock period)
- Upper bound for the speed of circuits which use these data
Clock resynchronization

- In each circuit, the PD compares external (CKE) and terminal-internal (CKI) clock edge positions.
- The internal clock phase is adjusted to compensate for the clock distribution three delay.
- CKE and CKI are synchronized.
Resynchronized outputs

- Driving the clock tree through the PLL, the switching time of output registers are synchronized with external clock, independently from internal clock delay.
Resynchronization with DLL

- No need for VCO, only phase adjustment
- The circuit is a Delay Lock Loop (DLL)
Lesson B7: PLL digital applications

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  - Clock multipliers
  - Resynchronization with DLL

- Clock-data recovery (CDR)
  - Self-synchronizing serial transmission
  - Embedded clock

- PSK demodulator
  - Example of embedded clock
  - Lock of phase-modulated signals
Clock-data synchronization

• When data and clock use two separate channels (wire, track, …), the different delays cause skew
  – The skew modifies timing relations
  – May cause violation of timing constraints (setup and hold)
  – The skew is the actual limit to data rate

• Solutions
  – Reduce and match delays
    » Matched lines, meanders, ..
  – Carry clock and date on the same wire
    » Clock embedding
    » Self-synchronizing codes and Clock-Data Recovery
    » Needs clock/data separation at destination
Embedded clock

• The timing information (clock) is mixed with data
  – Edges carry timing information

• Goal: guarantee maximum edge interval
  – Specific modulation at bit level (symbols)
  – Encoding techniques (maximum edge interval)
  – Increased number of edges → wider bandwidth

• Examples
  – Manchester encoding
  – Synchronous modulations
  – BxBy encoding
  – Bit stuffing
  – Synchronous protocols
Manchester encoding

- Phase modulation (phase steps $\pi$)
  - Symbol for 0: $H \rightarrow L$ transition
  - Symbol for 1: $L \rightarrow H$ transition
  - At least one edge in each bit slot
  - Bandwidth: max 2 edges/bit, $F_{max} = \text{BitRate}$

- Variations
  - MFM
  - M2FM: Manchester :2
MFM and M2FM codes

• MFM
  – Related with the bit sequence
  – 0: state change at Tbit end
  – 1: isolated: no change
    sequence: change in the middle of Tbit

• M2FM
  – Manchester :2
  – Same information
  – Reduced bandwidth: 1 transition/bit
  – More complex decoder
Summary of Manchester codes

a) BiΦ-L

b) BiΦ-M

c) MFM

d) M²FM
Spectrum of various codes

- More edges $\rightarrow$ more bandwidth occupation

![Graph showing spectrum of various codes with NRZ, MFM, and BiΦ curves.](image)
Synchronous modulations

- Integer number of carrier period in each bit slot
- Synchronous demodulation requires carrier recovery
- Clock can be derived from carrier
- Examples:
  - ASK/PAM (with residual carrier)
  - PSK (with phase shift at fixed positions in the period)
  - FSK (with integer number of carrier periods/bit)
BxBy encoding

- X-bit block replaced by a Y-bit block (with Y>X)
  - The new block guarantees
    » A minimum number of edges
    » DC level = 0 (or almost 0)
    » Reserved codes for commands/controls
  - Can be encoded NRZ (better bandwidth usage)
  - Increased bandwidth (same % as bit number increment)

- Most used
  - 4B5B
  - 8B10B
  - 64B66B
Example B4B5

- From 4-bit codes (16) to 5-bit codes (32)
- Redundancy used for:
  - New edges
  - DC removal
  - control characters

<table>
<thead>
<tr>
<th></th>
<th>0000</th>
<th>11110</th>
<th>1000</th>
<th>10010</th>
</tr>
</thead>
<tbody>
<tr>
<td>0001</td>
<td>01001</td>
<td>1001</td>
<td>10011</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td>10100</td>
<td>1010</td>
<td>10110</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td>10101</td>
<td>1011</td>
<td>10111</td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td>01010</td>
<td>1100</td>
<td>11010</td>
<td></td>
</tr>
<tr>
<td>0101</td>
<td>01011</td>
<td>1101</td>
<td>11011</td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td>01110</td>
<td>1110</td>
<td>11100</td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td>01111</td>
<td>1111</td>
<td>11101</td>
<td></td>
</tr>
</tbody>
</table>
Clock recovery

- Clock generator synchronized by signal edges
  - Requires minimum transition rate
Clock recovery circuit

- The clock oscillator can use a PLL

- The signal must have an adequate rate of transitions (edges), using
  - bit stuffing or coding (e.g. 8B10B)
  - Modulation (e.g. PSK 180°)
Data resynchronization: Altera

- Mercury EPLD
  - PLL multiphase clock generator (8)
  - Interpolation between clocks (1/56 Tck)
Clock/Data recovery example

- Altera Stratix (3 Gb/s)
Data resynchronization: Xilinx

- Two-phase clock generator, multiphase sampling
Data/clock recovery

- Multiphase sampling with resynchronization
  - Shift in the time domain without risk of metastability
Data/clock recovery

- Analysis of data transition position

![Diagram of data/clock recovery](image_url)
Data/clock recovery

• Select the correct-phase clock

– Similar to a clock-waveform correlator
– A standard correlator requires a faster clock (x 4)
Lesson C7: PLL digital applications

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• PSK demodulator
  – Example of embedded clock
  – Lock of phase-modulated signals
PSK modulation

- Carrier-synchronous modulation
- Phase jump 180°
Coherent PSK demodulators

• Coherent demodulators requires locking the PLL with a phase modulated signal.
  – How to phase-lock on a phase changing signal?

• Remove modulation
  – If $2\pi/N$ rotations, raise to power N
  – Lock on carrier $x N$

• Exploit some features of the modulation
  – Transitions in fixed positions
  – PSK - 180° example
PSK demodulator - operations

• Obtain pulses from transitions (A)
  – Always a transition in the middle of Tbit

• Filter the middle-Tbit pulses (C)
  – Block pulses at Tbit boundary: mask B

• Lock the pulse sequence with a PLL
  – Double-frequency VCO (E)

• Obtain signals with $\pi/2$ phase difference (B and D)
  – Complementary dividers

• Sample the input (or AM coherent demodulation)
Coherent PSK demodulator - signals

- Modulation
- Modulated signal
- Transitions
- Window for fixed transitions
- Fixed transitions
- Synchronous signal
- Dual frequency
- Demodulated out
Coherent PSK demod. – block diagram
Integrating demodulator

- Digital sampling: use a minimum part of the signal
  - 1 bit quantization
  - Single sample
  - Information loss, noise sensitivity

- Continuous evaluation
  - XOR and average over the period
    » Only quantization error
  - Coherent demodulation
    (reference signal) x (analog input signal),
    integrated over one period,
    final evaluation of the sign
    » Uses all information in amplitude and time domains
Message synchronization

• Special character at beginning of message (SOH, SYNC, …)
  – Symbol different from resting line
  – Similar to a Start Bit
  – Not usable in data field (or search disabled)
Synchronization sequences

- Autocorrelation function with a single maximum
  - PN sequences, Barker, Gold, ...

- Correlation circuits
  - Shift register with decoder on parallel outputs
  - Shift register with weighted summation of outputs
  - Analog correlator
  - Serial correlator

- Used in UMTS (descrambling) and GPS/Galileo

- Usable for bit synchronization and clock recovery
  - Multiple sampling + correlation
Parallel correlator

- Recognizes a pattern in the shift register
  - All bits must match
  - No error allowed
  - Used for short sequences

Find $61_H$
(0110 0001)

Synch out
Serial correlator

- Compares input and reference on each clock
- Counter of different bits (errors)
  - Can accept errors (threshold below total bit number)
  - Search for correlation maximum
Analog correlator

- Sum the shift register output with +1 weights
  - Can accept errors (threshold below total bit number)
  - Search for correlation maximum

- Can use multibit or analog samples
  - Better max positioning
Lesson C7 – Test questions

• List some applications of PLLs in digital circuits.

• Which are the benefits of clock resynchronization in complex ICs?

• Which are the benefits of clock embedding in a digital serial channel?

• Describe some techniques to embed clock and data in the same signal.

• Which modulations or encoding allow clock recovery from data?

• Which techniques can be used for digital phase demodulation?