Lab 7: DELTA AND SIGMA-DELTA A/D CONVERTER

Goal

The goals of this experiment are:
- Verify the operation of a differential ADC;
- Find the frequency and amplitude range of signal handled by a Delta converter, and the relation with clock rate;
- Find the frequency and amplitude range of signal handled by a Sigma-Delta converter;

Instruments and equipment

- +5 and -5 V power supply
- audio signal generator
- scope
- frequency meter
- multimeter
- breadboard

Specifications

Input signal (sinewave) frequency range: from 10 Hz to 500 Hz,
Maximum input signal level: 5 Vpp.
sampling rate from 3 kHz to 30 kHz,

Part list

- CD4013, and TL081 or TL082 Op Amp;
- passive devices (from design section).

Most common problems and mistakes

- Remember that in CMOS circuits inputs cannot be left floating. Every input pin must receive a voltage corresponding to a correct logic state.
- When setting the signal generator output level, remember that no IC pin can accept a voltage external to the supply range (in this case +/- 5V). Turn ON power supply before applying the clock.
- Values of resistors at Op Amp inputs must be selected to limit offset. Loads at Op Amp outputs should not exceed the maximum output current.
Clock source

Delta and Sigma Delta converters use a clock signal (CK). Since the signal generator available on the lab bench is used for the input signal, the converter clock is provided by an astable circuit based on an Op. Amp.

The circuit uses a hysteretic threshold comparator, built around an Op Amp: the TL082 (dual version; also TL081 or TL084 can be used). The Op. Amp. should use a symmetric power supply of +5V (respectively Vdd and Vss). These same supply voltages can be directly used for the CMOS CD4000 ICs (the CD4013 in this case), since they can work with supply voltage up to 15V. In this way the voltage levels from the clock generator are compatible with logic inputs.

In each half-period, the voltage on the capacitor starts from one of the thresholds and moves exponentially towards the output voltage. As the second threshold is crossed, the output sign is inverted and the capacitor discharges towards the new output level.

Find the value of C1 which gives the specified frequency range (3 - 30 kHz +/- 20%), with R3 + P variable from 10kΩ to 110kΩ (fixed 10k resistor, 100 k potentiometer connected as variable resistance).

The same clock generator is used both in Delta and Sigma-Delta converters.

Wire and test the clock generator before wiring other parts of the circuit.

Integrator

The integrating unit for the Delta converter uses a low-pass RC cell.

The Delta-Sigma converter uses an active integrator, based on an Op Amp. It uses the TL081 or TL082 circuits (the same device previously used as comparator).
Complete differential ADC (Delta type)

The first part of this experiment consists of measurements on a differential converter, using a a Flip-Flop for digital sampling after the voltage comparator. While the “classic” differential converter uses a switch to sample the comparator output, this circuit uses a D-FF. The output is a sequence of levels (positive or negative steps), instead of pulses. The reconstructed signal is the integral of a sequence of steps, that is a sequence of triangular waves (integral of steps).

The measurements include a check of operation with DC and sinewave input signals, and of dynamic parameters (idle noise and overload condition), for various amplitude and frequency of input signal.

The complete diagram of the circuit is in figure 2.

![Differential converter diagram](image)

The two Op Amps can belong to a single TL082 IC. Use the same power supply voltages of the CD4013 flip-flop (symmetric supplies +/- 5V). In this way the comparator output is directly compatible with logic circuit input.

All inputs of the unused flip-flop in the CD4013 must be connected to low level (–5V).

Design

The R4 resistor provides the input bias current for the Op. Amp., even with Va open or with capacitive input coupling. The value must be such to limit offset error, without placing high load on signal input.

The lowpass loop filter (R5-C2) and the reconstruction filter (R6-C3) are identical. R5 has constraints similar to R4. Design the filters to get a quantization step ($\gamma$) about 100mV, with a 20 kHz clock.

Verify if the converter can operate over the full range specified for input signal voltage and frequency, without introducing overload distortion.
Measurements

1. As first step wire only the clock generator circuit (A2, R1, R2, R3, C1). Apply +/-5V power supply and verify the output waveform (squarewave, about +/- 4 V) and frequency range. Set the frequency at 20 kHz.

2. Mount the remaining part of the circuit. The CD4013 FF ground pin (Vss) should go to – 5V, and the power supply pin (Vdd) to + 5V (with this configuration the logic circuit provides VH = +5V and VL = -5V). Connect to the low state voltage (-5V) the Set and Reset inputs of the used FF, and input pins (Set, Reset, Clock, Data) of the one not used.

3. Leave VA open, and measure with the scope the voltage at VD, VB and on the inverting input of A1.
   - Which is the operating state of the converter in this condition?
   - Which converter parameter can be measured?

4. Connect on VA the signal generator, set for sine output, 1 Vp, and check the reconstructed signal.
   - How is this last modified as the input frequency increases?
   - Which is the maximum frequency for correct conversion?
   - Which the minimum?

5. Change the amplitude of input sine signal, analyze and discuss the relation between maximum signal frequency and signal amplitude.

6. Change the clock rate; analyze and discuss relations between input signal level and frequency, and clock rate.

7. Which converter parameter becomes worse as the input level decreases?

8. Describe how the circuit can be modified to improve the quality (higher SNR) for the reconstructed signal.
Sigma-Delta differential ADC

The diagram of a first order Sigma-Delta differential converter is in figure 3.

The circuit is similar to Delta differential. Now the integrator is placed before the 1-bit quantizer (voltage comparator), and receives the sum of input and feedback signals. The new circuit can be obtained from the previous one with only small changes on the wiring (C2, R4, input pin + of the comparator A1).

![Diagram of a first order Sigma-Delta differential converter.](image)

Fig. 3 – Order I Sigma-Delta differential converter.

The circuit uses the same clock generator and supply scheme (+/- 5V). The CD4013 flip-flop receives symmetric supplies, and the comparator output is compatible with logic circuit input. All inputs of the unused flip-flop in the CD4013 must be connected to low level (~5V).

Use for Op Amp and comparator the TL081 or TL082 IC, with the same supply of the CD4013.

**Design**

The specifications for design are:

- input signal dynamic range: +/-3V
- clock frequency: nominal 20kHz (variable in the previously indicated range)
- maximum signal frequency: 500Hz

The design must define the values of passive components. A design guide (in Italian) is available in the 2006 course website: “Progetto di un convertitore Delta-Sigma”.
Measurements

1. Modify the circuit from Delta to Sigma-Delta differential.

2. Connect \( V_A \) to ground, and measure (with the scope) the voltages at \( V_u1 \) and \( V_u2 \).

3. Connect \( V_A \) to a DC voltage in the range +/- 5V (use a potentiometer connected between the + and – 5 V supply lines).
   - Verify and discuss the \( V_u1 \) and \( V_u2 \) signals.
   - Which is the DC dynamic range of the converter?

4. Connect on \( V_A \) the signal generator, set for sine output, 2 Vp, and check the output signal.
   - Describe the signals at \( V_u1 \) and \( V_u2 \) with changing frequency.
   - How can we evaluate the “quality” of the converter?

5. Change the sine input level, and verify the relationship between maximum frequency accepted by the A/D and signal amplitude

6. Which converter parameter becomes worse as the input level decreases?

7. Change the clock rate; analyze and discuss relations between input signal level and frequency, and clock rate.

Lab report

Start with a (short) summary of the design procedures. Provide a table with all information required for component acquisition (type, value, other parameters, …). At least for some of them give the reference (part number) for a commercial provider (e.g. Digi-Key, RS, …).

Draw complete schematic diagram, with component labels pointing to the table above.

For the other sections follow the instructions of the general lab guide.