HIGH SPEED AND HIGH PRECISION ANALOG TO DIGITAL CONVERTER

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Introduction

Overview .................................................................2
Applications of High Speed ADCs.................................2
Selecting the Right ADC..............................................3
  • Voice – Band Recording .........................................3
  • Quantizer in delta-sigma converter............................4

Delta-Sigma Converter
Delta-Sigma Converter..............................................5
Delta-Sigma A/D Converter Architecture........................5
  • Delta-Sigma Oversampling A/D Converter Principle.......5
  • Matlab Simulink....................................................9
  • Higher-Order Single-Stage Converters.......................12

Usage of SAR and Delta-sigma ADC together Nowadays
Usage of SAR and Delta-sigma ADC together Nowadays........14
  • Example of combination of best features of SAR converters and sigma-delta ADCs.................................15
  • Example of converter devices for Delta Sigma...............16

Digital Filter..................................................................17
References....................................................................18
**Introduction:**

Digital signal processing methods fundamentally require that signals are quantized at discrete time instances and represented as a sequence of words consisting of 1’s and 0’s. In nature, signals are usually non-quantized and continuously varied with time. Natural signals such as air pressure waves as a result of speech are converted by a transducer to a proportional analog electrical signal. Consequently, it is necessary to perform a conversion of the analog electrical signal to a digital representation or vice versa if an analog output is desired. The number of quantization levels used to represent the analog signal and the rate at which it is sampled is a function of the desired accuracy, bandwidth that is required, and the cost of the system. Figure 1 shows the basic elements of a digital signal processing system. The analog signal is first converted to a discrete time signal by a sample and hold circuit.

![Diagram of Digital Signal Processing System](image)

**Fig.1: Digital signal processing system.**

The output of the sample and hold is then applied to an analog-to-digital converter (A/D) circuit where the sampled analog signal is converted to a digitally coded signal.
Applications of High Speed ADCs:

- The key requirement for the ADC is to achieve better ENOB for input frequencies. The sampling rate requirement thus becomes the major deterministic factor in choosing a proper converter architecture.

- A quantizer is a device that converts a continuous range of input amplitude levels into a finite set of discrete digital code words.

A quantizer can be uniquely described by its transfer function or quantization characteristic, which contains two sets of information: the first includes the digital codes associated with each output state, and the second includes the threshold levels which are the set of input amplitudes at which the quantizer transitions from one output code to the next.

Selecting the Right ADC:

Selecting the most suitable A/D converter (ADC) for our application is based on more than just the precision or bits. Different architectures are available, each exhibiting advantages and disadvantages in various data acquisition systems. The required accuracy or precision of the system puts us in a category based on the number of bits required. It is important to always design our system to allow for more bits than initially required: if an application calls for ten bits of accuracy, choose a 12 bits converter. The achievable accuracy of a converter will always be less than the total number of bits available.

Successive Approximation Register (SAR) converters typically range from 8 to 16 bits, while delta-sigma converters can achieve an accuracy of up to 24 bits.

As a result, in below statement we will explain why the delta-sigma converters are the good choice for having the high speed and precision A/D converter for Voice.
- **Voice – Band Recording**

The human ear can detect signals from roughly 20Hz up to 20KHz. If the application is telephone intercom system where high-fidelity audio is not a concern, 60-70 dB of dynamic range is sufficient. Based on these bandwidth and dynamic range requirements, either a medium speed (50-200Ksps) the delta-sigma converter would work in this application.

- **Quantizer in delta-sigma converter:**

Based on the locations of threshold level in ADCs, quantizers can be divided to two categories: uniform and non-uniform (Figure.2). The thresholds of uniform quantizers are evenly distributed while in non-uniform quantizers thresholds locations match the probability density function of the incoming signal Voice.

![Quantizer transfer characteristics](image)

**Fig.2:** Quantizer transfer characteristics (a) uniform quantizer. (b) non-uniform quantizer.
Delta-Sigma Converter:

For digital systems to interact with analog signal sources, such as voice, data, and video, the role of analog-to-digital interface is essential. In voice data processing and communication, an accurate digital form is often desired to represent the voice. Due to the large demand of these systems, the cost must be kept at a minimum. All these requirements call upon a need to implement monolithic high resolution analog-to-digital interfaces in economical semiconductor technology. However, with the increasing complexity of integration and a trend of reducing supply voltage, the accuracy of device components and analog signal dynamic range deteriorate. It becomes more difficult to realize high resolution conversions by conventional Nyquist rate converter architecture. Compared to Nyquist rate converters, the oversampling converters use coarse analog components at the front end and employ more digital signal processing in the later stages. High resolution conversions are achieved by trading off speed and digital signal processing complexity, both of which can be easily realized in modern VLSI technology.

The oversampling A/D converter and Nyquist rate converter are compared in Fig.3. A non-oversampled A/D converter has an anti-aliasing low-pass filter in the front.
The anti-aliasing filter attenuates high-frequency components buried in the analog input and prevents them from being aliased into the signal frequency band. Because the converter is sampled at the Nyquist rate, which is twice the input signal bandwidth, the anti-aliasing filter’s transition band must be very narrow and its stop-band must have enough suppression of the out-of-band noise. This requirement makes the filter very complex and adds to the complexity that a non-oversampled A/D already has.

Delta-Sigma A/D Converter Architecture

- **Delta-Sigma Oversampling A/D Converter Principle**

The structure of a first-order delta-sigma converter is shown in Fig. 4. The input signal is
Fig. 4: The modulator of a first-order delta-sigma converter. T is the sampling period and n is the index.

sampled at a frequency $f_s$ ($T = 1/f_s$). A feedback signal from a 1-bit D/A converter is subtracted from the input and the residue signal is accumulated by an integrator. The output of the integrator is quantized to generate a 1-bit digital stream. This digital output sets the sign of the feedback. If the digital output is 1, it feeds back a large negative signal to subtract from the input signal. The net effect of the feedback loop is to keep the output of the integrator small so that the output digits always track the amplitudes of the input signal.

Quantization is a nonlinear process and the feedback mechanism makes the noise highly dependent on the input signal spectrum.

Useful information can still be obtained by linearizing the quantization process. The noise component is approximated by white additive noise uniformly distributed up to half of the sampling frequency. This approximation is valid because over a long period of time, the input to the quantizer will spread over a large number of values and appear to be quasi-random, so the noise introduced is quasi-random as well. Similar to a non-oversampled A/D converter, the rms value of the noise is $\sigma^2_{\text{rms}} = \Delta^2/12$, where $\Delta$ is the quantization step. When the quantizer is sampled at $f_s$, the noise power is sampled into a frequency band:

$0 \leq f < f_s/2$ and its spectral density is:

$$Q(f) = \sqrt{2} \cdot \sigma_{\text{rms}}$$

(1)

where $f$ is normalized to $f_s$. 

$$\sigma_{\text{rms}} = \Delta^2/12$$
The delta-sigma converter can be generalized as shown in Fig. 5. The forward path is modeled:

\[
x(n) \xrightarrow{B(z)} Q \xrightarrow{C(z)} y(n)
\]

**Fig.5: General feedback system.**

by transfer function \( B(z) \) plus the noise, and the feedback path can be modeled by \( C(z) \). The system output and input transfer function is governed by:

\[
Y(z) = \frac{B(z) \cdot X(z) + Q}{1 + B(z) \cdot C(z)}
\]  

(2)

To achieve high-resolution A/D conversion, the system needs to convert the input signal within a specified frequency bandwidth and minimize the noise component in that band. One method is to pass the signal component and block the noise component. This can be expressed as:

\[
Y(z) = X(z) + H_{ns}(z) \cdot Q
\]

(3)

where the input \( X(z) \) passes through the system, but the quantization noise is modified by a noise-shaping function \( H_{ns}(z) \).

Comparing these equations; to achieve the noise-shaping effect, the system in Fig. 5 needs to have the following property:

\[
\begin{align*}
C(z) &= 1 - \frac{1}{B(z)} \\
B(z) &= \frac{1}{H_{ns}(z)}
\end{align*}
\]

(4)

Now, we can see the delta-sigma A/D converter as a noise-shaping data converter.

The transfer function of the integrator in the forward pass is \( \frac{1}{1-z^{-1}} \); the D/A converter in the feedback path is equivalent to a delay element and its transfer function is \( z^{-1} \). They satisfy the
relation required by a noise-shaping converter in previous equation. Therefore, its noise-shaping function $H_{ns}(z)$ is:

$$H_{ns}(z) = \frac{1}{B(z)} = 1 - z^{-1}$$

(5)

which is a highpass filtering function. The amplitude of its response is:

$$|H_{ns}(z)| = |1 - z^{-1}| = 2 \sin(\pi f)$$

(6)

here $f$ is the normalized frequency with respect to $f_s$. This function is plotted in Fig.6. As shown in the figure, the noise is evenly distributed across the frequency, before applying the noise shaping function. The noise power in the signal band is the area of a region highlighted by the grey color underneath the flat line. After applying the noise-shaping function, the noise in the signal band is suppressed to a much lower level and the total noise power left (dark grey region) is much smaller than the original noise power. The high-frequency noise portion will be filtered by the digital filter. Therefore, the signal-to-noise ratio of the converter is greatly enhanced. Quantitatively, the noise power left in the signal band is the integration of its spectrum up to signal bandwidth $f_b$ as:

$$N^2 = \int_0^{f_b/f_s} (|H_{ns}(z)|^2 Q^2) \, df = \frac{2\Delta^2}{3 f_s} \int_0^{f_b/f_s} [\sin(\pi f)]^2 \, df$$

(7)

Where $Q^2$ is substituted for the noise spectral density in Eq. 1. In a delta-sigma converter the signal bandwidth is significantly lower than the sampling frequency. The resulting integration is:

$$N_q^2 = \frac{2\pi^2 \Delta^2}{9} \left( \frac{f_b}{f_s} \right)^3$$

(8)
Fig. 6: Plot of noise-shaping effect of the delta-sigma modulator comparing the noise power

• MATLAB SIMULINK:

1 - \( f = \text{linspace}(0, 0.5, 101); \)
2 - \( H = 2 \times \text{sin}(\pi f); \)
3 - \( \text{figure}(1); \)
4 - \( \text{plot}(f, \text{abs}(H), 'x', f, \text{abs}(H.^2), 'x', f, \text{abs}(H.^3), 'g', f, 1, 'k') \)
<table>
<thead>
<tr>
<th>f</th>
<th>Columns 1 through 9</th>
<th>Columns 10 through 18</th>
<th>Columns 19 through 27</th>
<th>Columns 28 through 36</th>
<th>Columns 37 through 45</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.0050 0.0100 0.0150 0.0200 0.0250 0.0300</td>
<td>0.0450 0.0500 0.0550 0.0600 0.0650 0.0700</td>
<td>0.0900 0.0950 0.1000 0.1050 0.1100 0.1150</td>
<td>0.1200 0.1250 0.1300</td>
<td>0.1350 0.1400 0.1450 0.1500 0.1550 0.1600</td>
</tr>
<tr>
<td>0.0050 0.0100 0.0150 0.0200 0.0250 0.0300</td>
<td>0.0450 0.0500 0.0550 0.0600 0.0650 0.0700</td>
<td>0.0900 0.0950 0.1000 0.1050 0.1100 0.1150</td>
<td>0.1200 0.1250 0.1300</td>
<td>0.1350 0.1400 0.1450 0.1500 0.1550 0.1600</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>Columns 1 through 9</td>
<td>Columns 10 through 18</td>
<td>Columns 19 through 27</td>
<td>Columns 28 through 36</td>
<td>Columns 37 through 45</td>
</tr>
<tr>
<td>0</td>
<td>0.0314 0.0628 0.0942 0.1256 0.1569 0.1882</td>
<td>0.2195 0.2507</td>
<td>0.2818 0.3129 0.3439 0.3748 0.4056 0.4363</td>
<td>0.4669 0.4974 0.5277</td>
<td>0.5580 0.5881 0.6180 0.6478 0.6775 0.7069</td>
</tr>
<tr>
<td>0.0314 0.0628 0.0942 0.1256 0.1569 0.1882</td>
<td>0.2195 0.2507</td>
<td>0.2818 0.3129 0.3439 0.3748 0.4056 0.4363</td>
<td>0.4669 0.4974 0.5277</td>
<td>0.5580 0.5881 0.6180 0.6478 0.6775 0.7069</td>
<td></td>
</tr>
</tbody>
</table>

Table.1: Frequency and transfer function of noise-shaping
For a sine wave input, the maximum signal amplitude is \( \frac{A}{2} \) and its average power is \( \frac{A^2}{8} \).

\[
\frac{S^2}{N^2} = \frac{9}{16\pi^2} \left( \frac{f_s}{f_b} \right)^3
\]

(9)

This gives a peak signal-to-noise ratio (SNR) as:

\[
SNR = 10 \log_{10} \left( \frac{S^2}{N^2} \right) = 20 \log_{10} \left( \frac{3}{\sqrt{2\pi}} \right) + 9 \log_2 M (dB)
\]

(10)

\( M \) is an important parameter called the oversampling ratio, defined as the ratio of the sampling frequency over the Nyquist sampling frequency \( 2f_b \). From this expression, we can see that we can get 9 \( dB \) of increase in SNR for every doubling of the sampling frequency. This corresponds to 1.5 bits. For example, if \( M = 128 \), we have 11.5 bits more resolution than sampling at the Nyquist rate.

This method allows a high resolution A/D conversion by using only a one-bit quantizer.
We can see that higher resolution is achieved by trading off the input signal bandwidth. In order to get 1.5 more bits, the bandwidth has to be cut by a half in this structure. To have a more favorable resolution and bandwidth trade-off, we can go to higher order delta-sigma converters.

**Higher-Order Single-Stage Converters**

In the first-order delta-sigma converter, the noise-shaping function is \( H_{ns}(z) = \frac{1}{1-z^{-1}} \).

Higher order converters can allow the noise-shaping function go up to \( L \)th power, given as:

\[
H_{ns}(z) = \left(1 - z^{-1}\right)^L
\]

(11)

where \( L \) is an integer greater than one. Thus, the magnitude of this noise-shaping function is:

\[
|H_{ns}(z)| = \left|1 - z^{-1}\right|^L = \left[2 \sin(\pi f)\right]^L.
\]

(12)

This function is also plotted in Fig. 6 for \( L=2 \). As seen in the figure, more noise from the signal band is blocked than with the first-order function. Integrating Eq. 11 over the signal band allows calculation of the SNR of an \( L \)th order delta-sigma converter as:

\[
\frac{S^2}{N^2} = \frac{3(2L+1)}{2^{2L+2} \pi^{2L}} \left(\frac{f_s}{f_b}\right)^{2L+1}
\]

(13)

which is equivalent to:

\[
SNR = 20 \log_{10} \left(\frac{\sqrt{3(2L+1)/\pi}}{\pi L}\right) + 3(2L+1) \log_2 M(dB)
\]

(14)

where \( M \) is the oversampling ratio. For every doubling of the sampling frequency, the SNR is increased by \( 3(2L+1) \)dB, i.e., \( L+0.5 \) bits more resolution. For example, \( L \) D 2 adds 2.5 bits.
Fig. 8: A plot of the resolution vs. oversampling ratio for different types of delta-sigma converters and Nyquist sampling converter.

and $L=3$ adds 3.5 bits of resolution. Therefore, compared to the first-order system, by employing a higher order delta-sigma converter architecture, the same resolution can be achieved with a lower sampling frequency, or a higher input bandwidth can be allowed at the same resolution with the same sampling frequency. Fig. 8 shows a plot of Eq. 14 comparing resolution vs. oversampling ratio for different order delta-sigma converters.

A second-order delta-sigma converter can be realized as shown in Fig.9 with two integrators. Higher order converters can be similarly constructed. However, when the order of the converter is greater than two, special care must be taken to insure the converter stability. More zeroes are introduced in the transfer function of the forward path to suppress the signal swing after the integrators.

Fig.9: Block diagram of a second order D-S modulator.
Other methods can be used to improve the resolution of the delta-sigma converter. A first-order and a second-order converter can be cascaded to achieve the same performance as a third-order converter, but with better stability over the frequency range. A multi-bit quantizer can also be used to replace the 1-bit quantizer in the architecture presented here. This improves the resolution at the same sampling speed. Interested readers are referred to reference articles.

In an oversampling converter, the digital decimation filter is also an integral part. Only after the decimation filter is the resolution of the converter realized.

**Usage of SAR and Delta-sigma ADC together Nowadays:**

To implement an Analog-to-Digital (AD) converter into a pure digital chip, a Delta-Sigma Digital-to-Analog (D/A) algorithm must be built in to work together with a successive approximation register (SAR). The slow conversion rate of Delta-Sigma D/A algorithm is the main limitation to the whole A/D converter for capturing high bandwidth periodic signals. In the following section, we will describe the proposed multi-pass method in detail, which can significantly enhance the apparent sampling rate of the whole A/D converter.

- **Example of combination of best features of SAR converters and sigma-delta ADCs**

  the device which is called CS556x/7x/8x; family of 16- and 24-bit analog-to-digital converters (ADCs) that claim to deliver the higher-bandwidth, low-distortion performance of a SAR converter with the high-resolution, low-noise performance of Delta-Sigma ADCs. The combination of features provides designers of precision instrumentation, with a significantly higher level of measurement accuracy, lower noise and higher throughput.
The CS556x is said to provide a much higher level of noise suppression than SAR converters, resulting in higher accuracy conversions and reduced post-conversion processing while adding to the robustness of the system. It also offers exceptional differential non-linearity (DNL) error, which measures the accuracy of the ADC and is critical in control applications. The family features DNL error as low as ±0.04 LSB typical (CS5571), compared to ±1 LSB typical within SAR converters.

In addition, the single-clock latency digital filter allows conversion-rate switching of the input with no loss in throughput. With near-flat digital FIR filter characteristics, the CS556x product line achieves unrestricted, wide-bandwidth signal throughput usually seen only in higher-speed SAR converters — at resolutions up to 24 bits. With this flat filter, output data is a 1:1 representation of the input signal across the entire frequency range, up to the sampling rate of the converter. In comparison, most delta-sigma converters use sinc filters, which attenuate the signal at specific frequencies.

Other features include high-impedance buffered inputs that simplify external circuitry; fully differential inputs that provide the best possible noise rejection and dynamic accuracy with the ability to measure bipolar signals; and self calibration to ensure measurement accuracy over variations in supply and temperature.

A flexible serial interface eases connections to a variety of microcontrollers without external components (includes slave and self-sequencing master modes).

**Example of converter devices for Delta Sigma:**

- **MCP3551/3 Devices** are 2.7 v -5.5v low power, 22-bit delta-sigma analog to digital converter (ADC). The devices offer output noise as low as 2.5 $\mu V_{PP}$, with the total unadjusted error of less than 10ppm. These devices provide high accuracy and low noise performance for application where sensor measurements such as (pressure, temperature and humidity) are performed.
With the internal oscillator and high over-sampling rate, minimal external components are required for high-accuracy applications.

**Fig. 10: Block Diagram of MCP3551/3 Devices**

This product line has fully differential analog inputs, making it compatible with a wide variety of sensor, industrial control or process control applications.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Sample Rate</th>
<th>Effective Resolution</th>
<th>50/60 Hz Rejection</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP3551</td>
<td>13.75 sps</td>
<td>21.9 bits</td>
<td>50/60 Hz (simultaneous)</td>
</tr>
<tr>
<td>MCP3553</td>
<td>60 sps</td>
<td>20.6 bits</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Table 2: Device selection**

**Digital Filter:**

The MCP3551/3 devices include a digital decimation filter, which is a fourth-order modified SINC filter. This filter averages the incoming bit stream from the modulator and outputs a 22-bit conversion word in binary two's complement. When all bits have been processed
by the filter, the output code is ready for SPI communication, the RDY flag is set on the SDO/RDY pin and all the internal registers are reset in order to process the next conversion. Like the commonly used SINC filter, the modified SINC filter in the MCP3551/3 family has the main notch frequency located at \( f_S/(\text{OSR} \times L) \), where \( f_S \) is the bit stream sample frequency. OSR is the Oversampling Ratio and \( L \) is the order of the filter. For the MCP3551 device, this notch is located at 55 Hz. For the MCP3553 device, the main notch is located at 240 Hz, with an OSR of 128. (below Table). The digital decimation SINC filter has been modified in order to offer staggered zeros in its transfer function. This modification is intended to widen the main notch in order to be less sensitive to oscillator deviation or line-frequency drift. The MCP3551 filter has staggered zeros spread in order to reject both 50 Hz and 60 Hz line frequencies simultaneously (Fig.11).

<table>
<thead>
<tr>
<th>Device</th>
<th>Output Data Rate (t(_{\text{CONV}})) (Note)</th>
<th>Output Noise (μVRMS)</th>
<th>Primary Notch (Hz)</th>
<th>Sample Frequency (f(_S))</th>
<th>Internal Clock f(_{\text{OSC}})</th>
<th>50/60 Hz Rejection</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP3551</td>
<td>72.73 ms</td>
<td>2.5</td>
<td>55</td>
<td>28160 Hz</td>
<td>112.64 kHz</td>
<td>-82 dB min. from 48 Hz to 63 Hz, -82 dB at 50 Hz and -88 dB at 60 Hz</td>
</tr>
<tr>
<td>MCP3553</td>
<td>16.67 ms</td>
<td>6</td>
<td>240</td>
<td>30720 Hz</td>
<td>122.88 kHz</td>
<td>Not Applicable</td>
</tr>
</tbody>
</table>

Table. 3: Data Rate, Output Noise and Digital Filter Specification by Device

Fig.11: Frequency
References:


