Interconnections for High-speed Digital Circuits

Lesson 1: Introduction

Goal

Any electronic system consists of subsystems, which carry out specific functions and exchange results and other information. Proper operation is based on the correctness of the functions and of the information transfer. This last relies on correct interfacing among subsystems, in static and dynamic conditions, and can be compromised by signal degradation and by disturbances generated either outside or inside the system itself.

As the speed of logic circuits continues to go up, the skills required to design reliable digital system include a good understanding of the analog behavior of signals and of electromagnetic wave propagation. As the gate delays become comparable with the travelling time of electromagnetic waves over a few cm, wires and PCB tracks must be treated as transmission lines.

After this course you will know how to connect digital devices, understanding how to get maximum transfer speed, and how to deal with the factors which limit the speed of digital systems.

Content and organization

The Interconnections for high-speed digital circuits course is structured in 5 lessons:

Introduction
Goal of the course, class of systems considered in the following lessons, and methodology used.
Review of static interfacing for digital circuits.

Interconnection models
Reference model for interconnection analysis. RC models; definition of interconnection parameters.
Refined lumped-parameter models.

Transmission lines models
Distributed-parameters models Transmission lines parameters, critical length, reflected waves.

Analysis techniques
Lattice diagram. Use of simulators; (Matlab), examples of results.

Design Guide for Interconnections
Incident Wave Switching, Line Termination Circuits, High Current Drivers and Series Termination, Multi-point and Bused Line.

Prerequisites

To follow these lessons you must already be familiar with:
- Circuit theory: R-C cells, transient response,
- Internal structure of digital logic circuits,
- Static electrical parameters of logic circuits,
- Function and use of basic instruments (pulse generator, oscilloscope).

Learning material developed for COREP within the EU project “Distance Learning Materials in Microelectronics for Materialists” (MIND), coordinated by the Bolton Institute of Higher Education (UK).

MIND first edition: February 2000
Revised October 2013 (rev j)
Acknowledgements

The photographs have been taken by the author during the laboratory exercises of courses held at the Politecnico di Torino. Some of the drawings are screen capture from simulators developed by the author, or from the "Elettronica II" CD-ROM developed by the author for COREP.

These notes were first developed within the EU project MIND, coordinated by COREP (200x).

Summary

The first lesson answers to the following questions:

- Which kind of systems are addressed?
- What does “dynamic interfacing” mean?
- Which kind of signals are here analyzed?
- Which are the relevant static parameters of digital logic circuits?

References

The parameters of digital circuits are described in:

J. Millman, A. Grabel: Microelectronics
Section 6.

A reference textbook with both general and detailed discussion of interconnections and signal integrity problems is:

H.W. Johnson, M.Graham:

The same author has a web site, with several articles and pointers:

http://www.signalintegrity.com/ftrecord.htm

Other more specific references are provided in each lesson

For this lesson, the related sections in the reference book are: 1.1, 1.2, 2.1, 2.2, and 2.3.

Examples of dynamic interfacing problems

1) Spikes and temporary faults appear at the output of a combinatorial circuit. The reason is that the change of logic state is sensed with different delays by logic circuit connected to the same signal. This may cause transient combinations of logic states which were not taken into account in the design process.

2) Fig 1.1 shows two microprocessors driven by the same clock signal. That means they should run synchronously, without problems related with marginal timing, such as metastability. In the real circuit, for some combinations of temperature and supply voltage, the system exhibits random errors for microprocessor 2. Swapping the devices has no effect, therefore the problem is related with the socket, not with the device.

Fig 1.1 Clock distribution to a couple of microprocessors.

The random errors are caused by synchronization problems (metastability) in the information exchange among the two microprocessors.

The solution is a redesign of the clock distribution circuit as in fig 1.2, taking into account transmission line effects. This can guarantee the timing margins for the synchronous circuits of the two microprocessors.

Fig 1.2 Improved clock distribution.
3) A full-rack length (49 cm) backplane is equipped with boards using 74F245 transceivers towards the bus, as in fig 1.3. Backplane signals on the scope exhibit high signal distortion (figure 1.4). Moreover, the bus interfaces have rather high power consumption.

Understanding the problem enables the designer to select the proper logic family for the drivers, thus achieving better waveforms, and reducing the power consumption.

IC technology and signal integrity

The microelectronic technology allows to put several million devices (transistor) on a single die, but similar advances did not occur in interconnection capability. Namely, the number of devices in a single IC scales with the square of the (chip size)/(device size) ratio ($S/\lambda$), while standard interconnection, being placed on the die boundary, scale linearly towards the same parameter. The two parameters are plotted in figure 1.5. Therefore, in the design of complex high-performance systems, we have to face an interconnection bottleneck.

This communication bottleneck is addressed by increasing the speed (bit rate) on external interconnections, and by increasing the number of pins. But higher speed means higher $dV/dt$ on I/O pins. This requires high currents to charge/discharge parasitic capacitors, and the effect is multiplied by the increase in the number of I/O pins. Higher currents mean more noise towards other circuits and systems, and careful design of interfaces is required to sustain the nominal speed of digital circuits in real systems.

Surface mount technology (figure 1.6) and new packaging techniques which reduce the size of devices and systems, and reduce parasitics by moving interconnection points from the boundary to any die position (e.g. BGA and flip-chip) help to deal with these problems. Also Low Voltage (LV) logic families, which reduce the $\Delta V$ between logic states help to limit EMI (and power consumption), at the expense of reducing noise margin and therefore increasing their susceptibility (sensitivity to external interference).

Fig 1.3 Loaded backplane bus.

Fig 1.4 Waveforms on a high speed digital interconnection.

Fig 1.5 Different rate of improvement for IC complexity and interconnection capability.

Fig 1.6 Surface mount packages (division on the top are 1 mm. each)
### Speed and distance

To evaluate the actual speed of information transfer, we must consider that in actual systems each conductor (wire, track) has resistance, capacitance, and inductance. Therefore signal transmission delays (and hence the speed of operation) depend not only from logic gates, but also from interconnections. The information is carried by electric signals, which are associated to electromagnetic waves, moving at high but limited speed. As the time scale of system operation (defined by the clock period) becomes of the same order of magnitude of the time required by electrical signals to move across a system, conductors cannot be considered equipotential, and we must model wires and tracks as transmission lines. Table A gives the approximate distance traveled by electrical signals on PCB during one clock period (Electrical length of the clock), for some common clock rates.

<table>
<thead>
<tr>
<th>Clock rate</th>
<th>Clock period</th>
<th>Electrical length</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>1 μs</td>
<td>200 m</td>
<td>old microprocessors</td>
</tr>
<tr>
<td>10 MHz</td>
<td>100 ns</td>
<td>20 m</td>
<td>current low performance microcontrollers</td>
</tr>
<tr>
<td>100 MHz</td>
<td>10 ns</td>
<td>2 m</td>
<td>current medium performance microprocessors</td>
</tr>
<tr>
<td>500 MHz</td>
<td>2 ns</td>
<td>0.4 m</td>
<td>high performance microprocessors and DSPs</td>
</tr>
</tbody>
</table>

What must be actually taken into account is not the clock period, but the edge slope. The change from one logic state to the other requires a finite time (roughly corresponding to the rise time or the fall time of the waveform). In first approximation, the spectrum of a digital signal covers from DC to a frequency $F = 1/2t_{\text{r}}$. Current high speed circuits, with rise/fall time below 1 ns, have significant components at frequencies above 500 MHz. The frequency content depends on edge steepness, not on repetition rate.

If the signal has to travel over some distance, devices tied to the same node (that is connected by a wire, or a PCB track) may sense different logic states. This effect is completely hidden in the conventional "logic diagrams", which assume that all logic circuits tied to a node sense the same state at the same time.

The rise/fall time of current logic devices is about 1 ns; that means only wires shorter that 20 cm can be considered a single "node".

These data shows how for most of modern high speed logic families: the interconnection delay and the transmission line effects interact with pure logic behavior of gates, and can cause false signalling. These effects put upper bounds on the speed of logic systems: even if the pure logic could run at infinite clock rate, the wiring introduces limits, as discussed in the following lessons.

### Digital signals: Static interfacing

The digital signals actually consist of analog voltages (and sometimes currents), which represent the logic state of logic variables (usually binary). Voltage and currents are defined as in fig 1.7.

![Fig 1.7 Two interconnected digital devices.](image)

The mapping between logic states and analog voltages is defined by the static electrical parameters.

<table>
<thead>
<tr>
<th>Logic State</th>
<th>Output electrical parameters:</th>
<th>Input electrical parameters:</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>$V_{OL}$, $I_{OL}$</td>
<td>$V_{IL}$, $I_{IL}$</td>
</tr>
<tr>
<td>HIGH</td>
<td>$V_{OH}$, $I_{OH}$</td>
<td>$V_{IH}$, $I_{IH}$</td>
</tr>
</tbody>
</table>

The static compatibility conditions (visualized in fig 1.8)

$$V_{IL} > V_{OL}$$ and $$V_{IH} < V_{OH}$$

guarantee that electrical levels are correctly recognized as logic states.

![Fig 1.8 Electrical compatibility chart.](image)

Since each input sinks/sources a current, and the current handling capability of outputs is limited, the static interfacing conditions include another relation:

$$I_{O\text{X}} > \sum I_{I\text{X}}$$

(the total current at driver output must be lower that the $I_{OH}$ or $I_{OL}$ specified by the manufacturer). This condition puts an upper bound on the number of inputs that can be connected to the same output. Even if most of current digital circuits use CMOS devices, with input currents practically 0 (and therefore there is no limit in a purely static situation), CMOS inputs are always dynamic loads (capacitance), and increasing their number brings to speed reduction, as discussed in the following lessons.
Digital signals: Dynamic interfacing

The behavior of digital signal in the time domain is defined by a set of timing parameters.

Rise time $t_R$ and fall time $t_F$ : time required by the signal to slew from 10% to 90% of total swing.

![Fig 1.9 Definition of rise and fall times.](image)

Propagation delays, $t_{PLH}$ and $t_{PHL}$ : respectively for LOW to HIGH and HIGH to LOW state changes. Figure 1.10a shows the input-output relationship for an inverter. The actual signals on a scope are in figure 1.10b.

![Fig 1.10a Definition of propagation delays.](image)

Correct operation of Flip-Flops and registers require compliance with minimum set-up time ($t_{SU}$) and hold time ($t_H$). When these limits are fulfilled, the output state changes with a propagation delay $t_P$ after the clock active edge.

![Fig 1.11 Timing parameters for a D-FF.](image)

Three-state buffers introduce enable and disable delays: $t_{EN}$ and $t_{DIS}$.

![Fig 1.12 Timing parameters for a 3-state buffer.](image)

In summary, the main timing parameters are:
- $t_{PLH}$, $t_{PHL}$, $t_R$, $t_F$ (for any logic circuit)
- $t_{SU}$, $t_H$, $t_P$ (for Flip-Flop)
- $t_{EN}$, $t_{DIS}$ (for 3-State outputs)

Signal waveforms are modified by amplitude noise and time jitter, which changes the voltage levels and the timing margins, and may cause errors in the information transfer.

In the following we shall analyze how digital systems can be designed in such a way to minimize these effects, while running at highest allowed speed.
Review questions

1) Dynamic interfacing addresses:
   - static compatibility of logic circuits,
   - power consumption of logic circuits,
   - time-domain behavior of logic signals and circuits,
   - correctness of Boolean operations performed by logic gates.

Static compatibility and power consumption are mainly related with DC parameters; Boolean operators determine the internal structure of logic circuits, not their interfaces.

2) Assuming a signal propagation speed of 0.6 c (c is the free-space propagation speed of the light), the "electrical length" of one clock period at 50 MHz is:
   - 36 mm, 1 m, * 3.6 m, 6 m.

0.6 c = 0.6 \times 300.000 \text{ km/s} = 180.000 \text{ km/s}

For a 50 MHz clock the period is 20 ns; the distance traveled in 20 ns is

180 \times 10^{-6} \text{ m/s} \times 20 \times 10^{-9} \text{ s} = 3.6 \text{ m}.

3) The "propagation time" (t_{PHL}) is defined as:
   - the time required by the voltage representing a logic state to change from \( V_{OL} \) to \( V_{OH} \)
   - the delay between input and output state change for a High-to-Low transition
   - the time required by the voltage representing a logic state to change from \( V_{OL} \) to 50% of \( V_{OH} \)
   - the time required by the voltage representing a logic state to slew from 10% to 90% of \( V_{OH} - V_{OL} \).

Propagation times represent the delay between input and output of a logic device. The index (HL or LH) indicates the direction of the state change.

4) The "rise time" (t_{R}) is defined as:
   - the time required by the voltage representing a logic state to change from \( V_{OL} \) to \( V_{OH} \)
   - the time required by the voltage representing a logic state to change from \( V_{OL} \) to 50% of \( V_{OH} \)
   - the time required by the voltage representing a logic state to go from 10% to 90% of \( V_{OH} - V_{OL} \)
   - the input-to-output delay of the receiver.

This is a definition – just learn it!

5) To explain the "set-up time" (t_{SU}) you could say:
   - the input D must be stable for at least t_{SU} before the clock active edge;
   - the input D must be stable for at least t_{SU} after the clock active edge;
   - the output Q will change with a delay at least t_{SU} after the active clock edge;
   - the minimum duration of the clock pulse is t_{SU};
   - the time required by the clock to slew from 10% to 90% of \( V_{OH} - V_{OL} \) is at least t_{SU}.

Flip-flops require time margins around the active clock edge to avoid metastability. The input data must not change during these time margins. The pre-edge time is the setup; post-clock margin is the hold time.

6) The "disable" (t_{DIS}) is defined as:
   - the time required by a three-state driver to exit from the high-impedance state,
   - the time required by a three-state driver to enter the high-impedance state,
   - the input-output delay in a three-state driver to exit from the high-impedance state,
   - the time required by the voltage at the output of a three state driver to slew from 10% to 90% of \( V_{OH} - V_{OL} \).

Due to internal parasitic and delays, a three-state driver requires some time to switch between active and not-active states. These are the enable and disable times.

7) With microelectronic technology evolution, the interconnection capability (that is the product between <number of signals> and <bit rate>)
   - increases faster than local processing power,
   - increases slower than local processing power,
   - increases at the same rate as local processing power,
   - decreases.

Processing power depends from the number of active devices (transistors), which goes up with the square of the (feature size)/(chip size) ratio. Interconnection capability (for standard packages) depends on how many active devices can be placed on the sides of the chip, that is increases linearly with (feature size)/(chip size).
Interconnections for high-speed digital circuits

Lesson 2: Interconnection Models

Summary

We shall start the analysis from simple linear models for driver/receivers and interconnections; this allows to define the parameters which describe the behavior of systems made by several interconnected logic devices.

This lesson answers to the following questions:
- Which is a suitable reference model for interconnection analysis?
- Which first-approximation models can we use for drivers and receivers?
- Which parameters can be defined for an interconnection?
- What are "lumped parameters" and "distributed parameters" models?

References

For this lesson, the related sections in the reference book are: 1.3 and 4.1.

Reference model for interconnection analysis

The reference model for interconnection analysis consists of a driver, interconnection, receiver chain as in figure 2.1.

Before entering the driver and after the output of the receiver we have logic states (0, 1).

Between the driver output and the receiver input we describe the system in terms of electrical quantities such as voltage and current, or devices such as resistors, capacitors, ...

For the driver-interconnection-receiver systems we can define several models, with increasing accuracy:
- linear models for driver and receiver,
- RC, LC, LRC models for interconnections,
- transmission line models for interconnections
- nonlinear models drivers and receivers.

The reference signal for the interconnection analysis is a logic state change, modeled as a voltage step generator inside the driver.

The electrical behavior of logic gates is specified by the static electrical parameters; these parameters define the static compatibility conditions previously defined.

Receiver model

The nominal transfer function of an inverting receiver is shown in fig. 2.2. Examples of real transfer function are in fig 2.3. The input voltage is interpreted as LOW or HIGH state depending on his level with respect to a threshold $V_{TH}$, which can have any value in the range $V_{IL}$ - $V_{IH}$.

The red and blue transfer characteristics in fig 2.4 represent inverting buffers with different thresholds (both within specifications, that is in the range $V_{IL}$ - $V_{IH}$).

When the input voltage $V_{IN}$ is in the $V_{IL}$ - $V_{IH}$ range, it is not possible to state if it is above or below $V_{TH}$ for all logic circuits of that family.
In this example when the input voltage $V_{IN}$ is within the $V_{IL} - V_{IH}$ range, the "red" and "blue" inverters A and B (with different threshold voltages) map the same input signal to different output states. Static interfacing conditions are violated, and a Data Split may occur.

Data split happens because of faulty or poor design, or because external noise modifies the voltage level on the interconnection.

Fig 2.5 The same input can be interpreted as different logic state.

On data split the digital circuits tied to the same node sense different logic states, the system is forced to a state not foreseen in the design phase (logic synthesis). In turn, it causes output errors or, for sequential circuits, unpredictable evolution or deadlocks.

The indetermination of $V_{TH}$ is one of the reasons for the presence of skew (time indetermination) on interconnections. From this analysis we found that something wrong may happen when the input voltage $V_{IN}$ lies in the $V_{IL} - V_{IH}$ interval. A first rule for digital interface design can be derived from this consideration:

The input voltage $V_{IN}$ should lie in the $V_{IL} - V_{IH}$ interval for the shortest possible time.

This goal can be achieved by acting on two parameters:

- The amplitude of the $V_{IL} - V_{IH}$ interval, which must be as small as possible. This amplitude depends on the tolerance of $V_{TH}$, that is on the logic family. Some devices, specifically designed as interfaces, have tight tolerance on $V_{TH}$, which corresponds to a narrow $V_{IL} - V_{IH}$ interval.
- The slew rate of signals: faster transitions (short $t_R$ and $t_F$) means that $V_{IN}$ stays in the $V_{IL} - V_{IH}$ range for shorter time. On the other hand, it means also higher current, more EMI towards other systems, and higher power consumption.

RC interconnection model

We shall use the reference model shown in figure 2.6. SA and SC are logic variables (0/1 or LOW/HIGH), while inside the driver/receiver and on the interconnection we analyze electrical variables ($V, I, R, \ldots$). The driver is modeled by a Thevenin equivalent circuit: a logic state change at SA becomes a voltage step on $V_A$, the receiver is modeled as a capacitor (this corresponds to C-MOS devices), and R-C circuits will be used for the interconnection.

Fig 2.6 Driver and receiver models for interconnection analysis.

A first approximation model for the interconnection is shown in fig 2.7; it is modeled as a single node; the capacitor $C_I$ corresponds to the parasitic input capacitance of the wire and of the receiver (which is actually a good approximation for CMOS inputs). The circuit is a first order low-pass cell and the step response at the receiver input is an exponential.

Fig 2.7 Direct connection of nodes B and C.

At $t = 0$ $V_A$ applies the voltage step, and the capacitor $C_I$ can be considered a short-circuit, therefore the nodes B and C are at ground potential.

$t = 0 \quad V_C = 0, \quad V_B = 0$

When the transient is settled ($t \to \infty$), the capacitor becomes an open circuit, and the voltage at nodes B and C corresponds to $V_A$

$t \to \infty \quad V_C = V_B = V_A$

The complete expression for of $V_B$ and $V_C$ is (fig 2.8):

$V_B = V_C = V_A (1 - e^{-t/\tau})$ with $\tau = R C$

Fig 2.8 Waveforms in the direct connection model.

Parameters of the interconnection
From this simple circuit we can define a first parameter to characterize an interconnection: the delay from state change at the driver and state change at the receiver, called transmission time $t_{TX}$ (figure 2.9). This delay depends from the parameters of the driver ($R_O$, output levels $V_{UH}/V_{UL}$), and of the receiver ($C_I$, threshold voltage $V_{TH}$), and corresponds to the value of $t$ for $V_B = V_{TH}$.

$$t_{TX} = c \ln \left( \frac{V_A}{V_A - V_{TH}} \right)$$

A visualization of the skew is in figure 2.10.

Refined models

To improve the accuracy we can add a series resistance $R_S$ to model interconnection wire resistance, as in figure 2.11.

The circuit is still a first order low-pass cell, but the threshold $V_{TH}$ is now crossed at different times in nodes B and C (figure 2.12). This time difference is another type of skew: even assuming that all parameters are fixed and known, the transmission time depends on the position of the receiver (node B or C).

To further increase the accuracy from these basic RC models we can add new circuit elements that represent with more detail of the interconnection structure (figure 2.13):

- a series inductance $L$, to take into account the wire/track inductance: $R_S - L - C$ model;
- a parallel conductance $G_P$ towards ground, to model dielectric losses: $G_P - R_S - L - C$ model;

Resistance, capacitance, and inductance are actually distributed along the whole length of the conductor; to improve the model accuracy the system can be divided into several short pieces (cells), with a R-L-C equivalent circuit for each of them. All these models are based on conventional circuit
Review questions

1) The "transmission time" $t_{TX}$ is defined as:
   - the time required by the voltage representing a logic state to change from H to L (or vice versa)
   - the delay from a state change at the driver and the sensing of that state change by the receiver.
   - the time required by the electric signal to travel from the driver to the receiver
   - the input-to-output delay of the receiver.

The logic state changes become voltage steps at the output of logic circuits. They are sensed by other logic inputs when the voltage crosses the logic threshold. Due to output resistance of drivers and parasitic capacitance of interconnections and receivers, the voltage step becomes an exponential, and reaches the logic threshold after a delay called transmission time.

2) Using a model with series resistance, parallel conductance (R and C), the logic threshold is crossed
   - first at the driver output (near end), then at receiver input (far end)
   - first at the receiver input, then at the driver output
   - at the same time at the driver and at the receiver

The voltage at the near end (driver side) raises faster than the voltage at the far end (receiver).

3) The skew time is:
   - the delay from the state change at driver input and voltage change at driver output
   - the delay from the voltage change at receiver input and state change at receiver output
   - the delay from a state change at the driver and the sensing of that state change by the receiver.
   - the difference between transmission time in various system conditions and/or positions in the interconnection

Receiver sense logic state changes after the transmission time, that is with a delay related with parasitic parameters, value of the threshold, position on the interconnection. The total variation of the transmission time is called skew.

4) Which of the following elements is not considered in the analysis of an interconnection (and does not affect the behavior of the interconnection):
   - the output circuit (driver)
   - the input circuit (receiver)
   - the logic operations performed by interconnected devices
   - the static electrical parameters

The transmission time and the skew depend on the electrical parameters of the driver and of the receiver. The logic operation is performed inside the device, and does not affect the parameters of the interconnection.

5) If $V_{IN}$ stays in the $V_{IL}$ - $V_{IH}$ range:
   - the driver can be damaged,
the receiver can be damaged,
- a data split may occur,
- the receiver output is blocked at $V_{AL}/2$.

The receiver threshold is somewhere in the $V_{IL}$ - $V_{IH}$ range; if the input voltage is in the same range, various receivers can take different decisions (High or Low) for the same input voltage. This causes inconsistent system state and data split.

6) For a RC interconnection model the transmission time $t_{TX}$ is:

- $t_{TX} = RC \ln \left( \frac{V_A}{V_A - V_{TH}} \right)$,
- $t_{TX} = RC$,
- $t_{TX} = RC \left( \frac{V_A}{V_A - V_{TH}} \right)$,
- $t_{TX} = RC \ln V_{TH}$.

The transmission time $t_{TX}$ can be computed by solving the equation:

$$V_B = V_{TH} = V_A \left( 1 - e^{-t/\tau} \right) \quad \text{with} \quad \tau = RC$$

For $t = t_{TX}$, $V_B = V_{TH}$ : substituting in the above equation:

$$V_{TH} = V_A \left( 1 - e^{-t_{TX}/RC} \right)$$
$$V_{TH} - V_A = - V_A e^{-t_{TX}/RC}$$
$$- \ln(\frac{V_{TH} - V_A}{V_A}) = t_{TX}/RC$$

Interconnections for high-speed digital circuits

Lesson 3: Transmission-line Models

Summary

In the previous lessons we modeled interconnections with lumped elements, such as resistors and capacitors, and defined the basic parameters, which define interconnection performance: the transmission time and the skew. Here we shall move to distributed-parameter models, which are a better representation of interconnections for high-speed logical devices.

This lesson answers to the following questions:

- What are "lumped parameters" and "distributed parameters" models?
- What is a loss-less transmission line?
- Why and when should we use transmission line modes?
- What is a reflected wave?
- How can we compute reflection coefficients?

References

For this lesson, the related sections in the reference book are: 4.2 and 4.3.

A more specific analysis of transmission line models for digital circuits is in:
Richard E. Matick
Transmission Lines for Digital and Communication Networks
IEEE Press, 1995

Transmission line models

In the previous lesson we defined cell-based lumped-parameter models (figure 3.1).

![Multiple-cell model](image)

Fig 3.1 Multiple-cell model.

Each cell models a piece of wire (or PCB track); as the length of this piece diminishes and the number of cells increases, the model approximation improves. For an infinite number of very small cells, the sequence turns into a distributed parameter model or transmission line (Fig 3.2).
The transmission line is a distributed parameter model for the interconnection. The parameters of the transmission line are the \( R, L, C, G \) values for unit length (here labeled \( R', L', C', G' \)), which in turn depends from the physical parameters (dimensions, materials, …).

**Loss-less transmission lines**

When the series resistance \( R_S \) and the parallel conductance \( G_P \) are 0, the cells include only reactive elements (figure 3.3), and no power is dissipated on the line. In these conditions \( Z_0 \) is real and we talk of **loss-less transmission line**. Loss-less transmission lines are a very good approximation for PCB tracks, coaxial cable, copper wires. In the following we shall always use loss-less lines.

For an analysis of transmission lines as interconnection, we shall define two parameters:
- the propagation speed \( U \)
- the characteristic impedance \( Z_0 \).

They depend from inductance and capacitance per unit length (1 meter) \( L' \) and \( C' \).

\[
\begin{align*}
U &= \frac{1}{\sqrt{L'C'}} \\
Z_0 &= \sqrt{\frac{L'}{C'}}
\end{align*}
\]

The characteristic impedance \( Z_0 \) corresponds to the \( v/i \) ratio in any point of the line. When the physical parameters (size, materials) are constant, the same applies to \( L', C' \), and therefore to \( Z_0 \).

For a transmission line of length \( l \) we can define a **propagation time** \( t_P \) (time required by electromagnetic waves to travel over the length \( l \))

\[
t_P = \frac{l}{U}
\]

The characteristic impedance \( Z_0 \) and the propagation speed \( U \) for some commonly used interconnection media are within the following ranges:

<table>
<thead>
<tr>
<th>Media</th>
<th>( Z_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coaxial cables (figure 3.4)</td>
<td>50 - 100 ( \Omega )</td>
</tr>
<tr>
<td>Flat cables (signal/ground pairs, figure 3.5)</td>
<td>100-300 ( \Omega )</td>
</tr>
<tr>
<td>PCB tracks (with ground plane, figure 3.6)</td>
<td>20 - 200 ( \Omega )</td>
</tr>
</tbody>
</table>

Wider tracks have higher capacitance and lower inductance, that is lower characteristic impedance \( Z_0 \) and lower propagation speed \( U \). The inverse occurs with narrow tracks or when the gap between track and ground is decreased (that is when the board thickness is reduced).

As the unit inductance \( L' \) increases (more narrow track) the characteristic impedance \( Z_0 \) increases and the propagation speed \( U \) decreases.
When many devices are connected to a track, the unit capacitance $C'$ is increased by the device parasitic (input and output capacitance). Also in this case the characteristic impedance $Z_0$ and the propagation speed $U$ decrease.

Critical Length

If the propagation time over an interconnection is far less than rise and fall time of signals, the conductor can be considered equipotential; in this case lumped-parameters RC models defined in lesson 2 can be used. When the propagation time is of the same order of magnitude as the transition time of logic circuits the interconnections must be modeled as transmission line.

For each logic family a critical length (related with transition times) can be defined: connections longer than this critical length must be modeled as transmission lines.

The table shows the values of critical connection length for various logic families.

<table>
<thead>
<tr>
<th>Logic Family</th>
<th>Maximum Connection Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTL</td>
<td>60 cm</td>
</tr>
<tr>
<td>ALS</td>
<td>25 cm</td>
</tr>
<tr>
<td>AS</td>
<td>6.5 cm</td>
</tr>
<tr>
<td>HC</td>
<td>45 cm</td>
</tr>
<tr>
<td>ABT</td>
<td>15 cm</td>
</tr>
</tbody>
</table>

Reference transmission line model

The reference model for interconnection analysis consists of a driver-line-termination system, as in figure 3.7. The line has no loss. The driver sends a step signal on the left end of the line (near end); at the other end (far end) the line is terminated on a resistance $R_T$. Other logic circuits can be connected at any position along the line.

**Fig 3.7** Reference model for transmission line analysis.

The open-circuit voltage of the line driver is a voltage step with amplitude $V_A$. $R_O$ is the internal output resistance of the driver.

The line is defined by two parameters:

- the characteristic impedance $Z_0$
- the propagation time $t_p = \frac{l}{U}$, where $l$ is the physical length of the line and $U$ is the propagation speed.

$V_B$ is the voltage at node B (driver output, left side of the transmission line, or near end)

$V_C$ is the voltage at node C, corresponding to the right side of the line or far end. The termination resistance is connected to this node. The line termination can be a specific component or the input of a receiver.

Line driving

Let us first consider a driver connected to a line of infinite length (figure 3.8).

**Fig 3.8** Driving an infinite line.

When the logic state at driver input changes (e.g. 0 to 1), a voltage step $V_{OL}$ to $V_{OH}$, simplified as 0 to $V_A$ appears at the driver output. The driver is loaded by the transmission line that is by a dynamic impedance $Z_0$. The actual step at node B is given by the partition of $V_A$ across $R_O$ and $Z_0$ (Figure 3.9):

**Fig 3.9** Equivalent circuit for line driving.

$$V_B = \frac{V_A R_T}{R_O + Z_0}$$

This is called first step or incident wave, and corresponds to the amplitude of the incident wave travelling on the line from the driver (left side) towards the termination (right end).

As long as there is no discontinuity on the transmission line, the wave continues to travel on the line towards the right side. If we connect at the far end a resistance $R_T = Z_0$ the incident wave is absorbed by the termination, and the whole line goes to a steady state with $V_C = V_B$. In these conditions the line is matched.

On any discontinuity of the characteristic impedance $Z_0$ (change in track width, or insulator thickness or material, lumped loads, ...), part of the energy travelling along the line goes through the discontinuity and the remaining part is reflected backward, generating a reflected wave (figure 3.10).
The two ends of the line usually represent the most significant discontinuity; a typical situation for instance could be:
- open line at the far end,
- low resistance termination at driver.

**Propagation and reflected waves**

On the line voltage and current propagate at speed $U$ in both directions. Signals going towards the right end (incident or progressive wave) are indicated by $v_1, i_1$; signals going towards the left side (reflected or regressive wave) are $v_2, i_2$. All these signals depend on time and position, that is:

$$v = v(t, x); \quad i = i(t, x);$$

and the $v/i$ ratio for each wave corresponds to the characteristic impedance $Z_0$:

$$v_1/i_1 = Z_0; \quad v_2/i_2 = -Z_0$$

The total voltage and current at time $t$ in the position $x$ are the sum of incident and reflected terms:

$$v(t, x) = v_1(t - x/U) + v_2(t + x/U); \quad i(t, x) = i_1(t - x/U) - i_2(t + x/U)$$

At the far end (termination $R_T$) Kirchoff and Ohm laws apply:

$$i_T = i_1 + i_2; \quad v_T = v_1 + v_2; \quad \frac{v_T}{i_T} = R_T$$

While along the line we have:

$$i_1 = \frac{v_1}{Z_0}; \quad i_2 = -\frac{v_2}{Z_0}$$

therefore we get:

$$i_T = i_1 + i_2 = \frac{(v_1 + v_2)Z_0}{Z_0}$$

$$v_T = v_1 + v_2 = \frac{(v_1 + v_2)R_T}{Z_0}$$

$$v_1 = v_1(R_T - Z_0)/(R_T + Z_0)$$

If we define a reflection coefficient $\Gamma$ as:

$$\Gamma = \frac{R_T - Z_0}{R_T + Z_0}$$

the backward (reflected) wave $v_2$ can be written as:

$$v_2 = \Gamma v_1$$

These relations apply also when the characteristic impedance changes (variation in track size or distance from ground, lumped loads, ...). To comply line equations on both sides part of the incident wave is reflected towards the near end, and the remaining part continues on the line with the new characteristic impedance. Therefore, a reflected wave builds up at any discontinuity, including the near end (at the driver), if $R_D$ is not equal to $Z_0$.

**A sample system**

We can now analyze a driver-interconnection-receiver system. The interconnection is a PCB track, which can be considered loss-less transmission line. The only discontinuities are at both ends:
a termination resistance $R_T$ at the far end (at the receiver input)
- the driver with equivalent output resistance $R_O$ at the near end

At $t = 0$ the output of the driver sees the line as impedance $Z_0$: the voltage at node B is the partition of $V_A$ among $R_O$ and $Z_0$ (figure 3.11). This is the first step (incident wave) with amplitude:

$$V_b = \frac{V_A Z_0}{R_O + Z_0}$$

This signal corresponds to the first incident wave $V'$, which moves forward on the line at speed $U$.

At $t = t_p$ the step reaches the end of the line (node C). The signal at the far end C comes from a generator $V_L$ with equivalent impedance $Z_0$ (the transmission line), therefore for the incident wave $v/i = Z_0$.

On the termination resistance $R_T$, $v/i = R_T$. If $R_T$ is different from $Z_0$, a reflected wave $V''$ arises in C; and propagates backwards from the termination towards the driver.

The amplitude of this reflected wave is

$$V'' = \Gamma_o V' = \frac{R_T - Z_0}{R_T + Z_0} V'$$

At $t = 2 t_p$ the reflected wave $V''$ comes back to the driver output (node B). Since the driver output resistance $R_O$ is different from $Z_0$, a new reflected wave $V'''$ is generated.

$$V''' = V'' \Gamma_o$$

with $\Gamma_o = \frac{Z_0 - R_O}{Z_0 + R_O}$, and travels left-to-right (from the near end to the far end).

The complete sequence is in figure 3.13.

The voltage in any position is the sum of all incident and reflected waves. The waveforms in B and C are a sequence of steps with amplitude related with $R_O$, $Z_0$, $R_T$. The steps occur at $t = 2 K t_p$ at the near end (B), and at $(2k + 1) t_p$ at the far end (C).

Two examples of $V_B$ and $V_C$ for different combination of $R_T$ and $R_O$ are in figure 3.14 (screen capture from a simulator). A sample scope display of the waveforms at nodes B and C (with open circuit for $R_T$ and $R_O >> Z_0$) is in figure 3.15.
**Review questions**

1) A distributed model for interconnection contains
   - a single lumped-element cell
   - at least 5 lumped-element cells
   - at least 100 lumped-element cells
   - *an infinite number of cells

Distributed models are built by increasing the number of cells in lumped parameter models. As the number of cells increases – for a given line length – the value of parameters (R, L, C) decreases.

2) The speed of electromagnetic waves in coaxial cables and PCB tracks is about (c = free-space speed of light)
   - \( \frac{2}{c} \)
   - \( 0.7 \, c \)
   - \( c \)
   - \( 1 \, c \)

This can be seen as a result from measurements or calculations from physical parameters.

3) For thinner tracks, the characteristic impedance
   - increases
   - decreases
   - does not change

The track and the ground plane makes a capacitor; when track width decreases, the size of the capacitor decreases. The characteristic impedance \( Z_0 = \sqrt{\frac{L}{C}} \) goes up when \( C \) decreases.

4) For wider tracks, the characteristic impedance
   - increases
   - decreases
   - does not change

The track and the ground plane makes a capacitor; when track width increases, the size of the capacitor increases. The characteristic impedance \( Z_0 = \sqrt{\frac{L}{C}} \) goes down when \( C \) increases.

5) For thinner insulator towards ground, the characteristic impedance
   - increases
   - decreases
   - does not change

The track and the ground plane makes a capacitor; when the separation between plates decreases, the value of the capacitor increases. The characteristic impedance \( Z_0 = \sqrt{\frac{L}{C}} \) goes down when \( C \) increases.
6) For tickers insulator towards ground, the characteristic impedance

- increases
- decreases
- does not change

The track and the ground plane makes a capacitor; when the separation between plates increases, the value of the capacitor decreases. The characteristic impedance \( Z_0 = \sqrt{\frac{C}{\mu}} \) goes up when \( C \) decreases.

7) A 10 cm interconnection in a logic system using HC circuits

- can be considered a single node
- must be handled as transmission line

The rise/fall time in the HC logic family is a few ns. The distance travelled by the electric wave in this time is 40-60 cm, higher than the interconnection length.

8) The amplitude of the first step, for \( V_A = 5 \text{ V} \), \( R_0 = Z_0 \) is:

- 1 V
- 2 V
- 2.5 V
- 5 V.

\[
V_B = \frac{V_A Z_0}{R_0 + Z_0}
\]

\[
V_B = \frac{5V Z_0}{2Z_0} = 2.5V
\]

9) The reflection coefficient \( \Gamma \) is given by:

\[
\Gamma = \frac{(R_T - Z_0)(Z_0 - R_T)}{(R_T + Z_0)(R_T + Z_0)} \\
\Gamma = \Gamma = \frac{(Z_0 - R_T)(R_T + Z_0)}{(R_T - Z_0)(R_T + Z_0)}
\]

This is the result of network analysis, computing the reflected wave as excess voltage required to comply Ohm’s equation on the line and on the termination.

10) For \( R_T = 100 \Omega \) and \( Z_0 = 50 \Omega \) the value of reflection coefficient \( \Gamma \) is:

- \( \Gamma = 1 \)
- \( \Gamma = -1 \)
- \( \Gamma = 0.6 \)
- \( \Gamma = -0.6 \)

Can be computed from

\[
\Gamma = \frac{(R_T - Z_0)(R_T + Z_0)}{(R_T + Z_0)(R_T - Z_0)}
\]

Interconnections for high-speed digital circuits

Lesson 4: Analysis techniques

This lesson describes some techniques that can be used to analyze simple transmission-line interconnection systems. Results for some exemplary cases are presented.

Summary

This lesson answers to the following questions:

- How can we analyze transmission lines with linear drivers and receivers?
- How can we analyze transmission lines with non-linear drivers and receivers?
- Which technique can be used to evaluate transmission time and skew with transmission line models?
- Can we use standard mathematical tools and electrical simulators to analyze transmission line systems?

References

For this lesson, the related sections in the reference book are: 4.4 and 4.5.

Transmission time and skew

Transmission time and skew keep the definition given in lesson 2. Instead of following an exponential, now the voltage on the line changes as a sequence of steps, corresponding to the sequence of reflected waves (Figure 4.1).

Fig 4.1 Waveforms at the near end (top trace) and far end of a transmission line driven by digital signals.

The transmission time \( t_{TX} \) and the skew \( t_K \) are still defined as for RC models, but now their value is expressed in multiple of the propagation time \( t_P \), that is as the number of steps required to reach and cross the threshold. Figure 4.2 shows the near-end and far-end waveforms for an interconnection with low-current driver and open-circuit termination (this is the most common case for digital circuits).
In the following sections we shall analyze some simple specific cases for the termination resistance, evaluating the transmission time and the skew.

Effects of termination resistance

For the first reflected wave, we can look at signals for three specific cases.

1. \( R_T = Z_0 \quad \Gamma = 0; \)

   The line is matched: the \( V/I \) ratio is equal to \( Z_0 \) both on the line and at termination; \( \Gamma = 0 \) and there is no reflected wave. In figure 4.3 the top trace represents the voltage at the near end (driver), and bottom trace is voltage at termination. Since there is no reflection, we observe a single step, respectively at \( t = 0 \) (node B, driver, top trace) and \( t = t_P \) (node C, termination, bottom trace).

   If \( V_{TH} > V_A / 2 \), in this configuration \( t_{TXmax} = t_P \), \( t_K = t_P \).

2. \( R_T = \infty \quad \Gamma = 1; \)

   The termination is an open circuit: since \( \Gamma = 1 \), the reflected wave has the same amplitude and same polarity of the incident wave (figure 4.4). At the near end (node B, top trace) we can see a first step (at \( t = 0 \)), and a second step (same amplitude) at \( t = 2t_P \). On the termination (node C, bottom trace) the incident and reflected wave add, and we see a single step with double amplitude.

   If \( V_{TH} > V_A / 2 \), in this configuration \( t_{TXmax} = 2t_P \), \( t_K = t_P \).

3. \( R_T = 0 \quad \Gamma = -1; \)

   The termination is a short circuit: \( \Gamma = -1 \), the reflected wave has the same amplitude but opposite polarity of the incident wave. (the total voltage at the termination C (a short circuit) is 0, therefore the sum of incident and reflected wave must be 0). At \( t = 2t_P \) the reflected wave comes back to the driver and cancels the voltage \( V_B \). The resulting waveform in node B is a \( 2t_P \) pulse (red line in figure 4.5).

   If \( V_{TH} > V_A / 2 \), in this configuration \( t_{TXmax} = 2t_P \), \( t_K = t_P \).

Fig 4.2 Comparison between lumped-element and distributed element models.

Fig 4.3 Waveforms at the near end (top trace) and far end of a transmission line with matched termination.

Fig 4.4 Waveforms at the near end (top trace) and far end of an open transmission line.

Fig 4.5 Waveforms on a transmission line with short-circuit at the far end.
**Lattice diagram**

To analyze the behavior of the driver-line-receiver system we can use the lattice diagram technique (figure 4.6).

The lattice diagram represents on the horizontal axis ($x$) the segment of line under analysis, and on the vertical axis the time ($t$), increasing towards the bottom.

The signal on the line is represented by a point, which moves in the (x,t) plane on straight lines with a slope depending from the propagation speed $U = x/t$. When the signal hits a discontinuity (such as line ends in this example), a reflected wave with an amplitude depending from the corresponding $\Gamma$ is sent backwards.

![Fig 4.6 Structure of a lattice diagram.](image)

The diagram represents the signal trajectory in the (x,t) plane, that is the (x,t) pairs that satisfy the wave equation. The amplitude of each reflected wave is given by the incident wave multiplied for the reflection coefficient. The total signal amplitude can be obtained by summing the amplitude of the reflected waves sequentially generated at each end. The v(t) waveforms corresponds to a vertical section of the diagram in the corresponding position (point P in this example). The various contributions sum as they arrive at that point (that is when the lattice crosses the vertical line).

**Examples of Real Lines**

The following drawings represent lattice diagrams for some sample cases. The upper-right window shows the waveforms at the near end and at the far end.

![Fig 4.7: $RT = \infty$ $\Gamma_T = 1$; $RG = Z_0$ $\Gamma_G = 0$;](image)

Fig 4.7: $RT = \infty$ $\Gamma_T = 1$; $RG = Z_0$ $\Gamma_G = 0$;

Both reflection coefficients are positive: the waveforms are a sequence of steps with the same polarity.
Simulation code

The simulator provided in the following analyzes the behavior of loss-less transmission lines using the wave equations and computing actual waveforms using the lattice diagram technique.

The program generates three drawings, showing respectively the signals at near end, far end, and an intermediate point, and a 3D views of voltage on the line versus time and position.

The simulator is written in Matlab language (by MathWorks company: www.mathworks.com). To run this code you need the Matlab 5 environment. You may copy the source code, and modify the line or termination parameters.

% This code generates time/position views of step waveforms on a transmission line
% usage of variables:
% t time
% x position
% y amplitude
% numeric parameters can be modified directly in the source code
% to simulate different operating conditions;

clear
Zo = 100;  % line imp
Rs = 220;  % source imp
Rt = 1150; % term imp
tp = 4;    % propagation delay over L
L = 8;     % line length
Tmax = 45; % max observed time
G = 0; T = 0; t = 0;
Gt = (Rt-Zo)/(Rt+Zo); % Gamma at termination
Gs = (Rs-Zo)/(Rs+Zo); % Gamma at source
% first propagation
for t = 1:tp+1
    for x = 1:L
        U(t,x) = F + G*As*((x/L)<(t/tp));
    end
end
G = U(t,x) - F;
F = U(t,x);
bounce = 1;
% reflections
while t < Tmax
    for t = (bounce*tp):((bounce+1)*tp+1)
        for x = L:-1:1
            U(t,x) = F + G*Gs*(((L-x)/L)<((t-bounce*tp)/tp));
        end
    end
end
end
G = U(t,x) - F;
F = U(t,x);
bounce = bounce+1;

for t = (bounce*tp):(bounce*tp+1)
for x = 1:L
U(t,x) = F + G*Gs*((x/L)<((t-bounce*tp)/tp));
end
end
G = U(t,x) - F;
F = U(t,x);
bounce = bounce+1;
end
T = t;

% drawing results
x=1:L;
t=1:T;
[X,Y]=meshgrid(x,t);

mesh (X,Y,U)
title ('View from termination: Gt = ',num2str(Gt), ' Gs =',num2str(Gs));
xlabel ('distance'), ylabel ('time'), zlabel ('amplitude')
view ([40, 30]) % view from termination
%print -dwinc

figure
mesh (X,Y,U)
title ('View from source: Gt = ',num2str(Gt), ' Gs =',num2str(Gs));
xlabel ('distance'), ylabel ('time'), zlabel ('amplitude')
view([-50, 30]) % view from source
%print -dwinc

figure
plot (t, U(t,1), 'w', t, U(t,L/3), 'r', t, U(t,L), 'g')
%print –dwinc

Two examples of results from the simulator are give in figure 4.11 and 4.12.

Figure 4.11 shows the time evolution of the voltage on the line at different positions for an interconnection with positive reflection coefficients at source and at termination. All steps are positive, and the voltage at any point of the line is a monotonic staircase.

Fig 4.12 shows the time evolution of the voltage on the line at different positions for an interconnection with positive reflection coefficient at termination and negative reflection coefficient at source. This situation corresponds to a high current driver connected to an open line (termination resistance much higher than characteristic impedance). Now steps invert direction on any bounce at the driver side. The waveform can oscillate, and cause multiple threshold crossing.
Review questions

1) When \( V_{TH} > V_A / 2 \), the maximum transmission time for a line matched at source and at termination is:
   - \( t_{TX_{max}} = 0 \),  \( t_{TX_{max}} = t_P \),
   - \( t_{TX_{max}} = 2t_P \), the system does not work.

   With matched source the first step is \( V_A / 2 \); due to matching at the far end (termination) this is also the final voltage on the line. The voltage on the line never crosses the threshold.

2) When \( V_{TH} < V_A / 2 \), the maximum transmission time for a line matched at source and at termination is:
   - \( t_{TX_{max}} = 0 \),  \( t_{TX_{max}} = t_P \),  \( t_{TX_{max}} = 2t_P \), the system does not work.

   With matching at source and at termination the first edge (incident wave) reaches the far end in \( = t_P \), and there is no further reflection. All points on the line are reached within this time.

3) In which configuration can the line voltage have multiple threshold crossings? (RO is the output resistance of the driver; Z0 the line impedance, RT the termination resistance)
   - \( RO >> Z_0, RT = Z_0 \),  \( RO > Z_0, RT = oo \),
   - \( RO << Z_0, RT = Z_0 \),  \( RO << Z_0, RT = oo \).

   Multiple threshold crossing occurs when line voltage oscillates; this requires the composition of waves with opposite polarity, which are generated by a negative reflection coefficient at source.
Incident wave switching

Incident wave switching (IWS) occurs when the receiver can sense the logic state change on the first step impressed to the line. To guarantee this condition, the first step must be higher than the threshold $V_{TH}$, and this means $Z_0 >> R_O$. This can be obtained by lowering the output resistance $R_O$ (that is using high-current drivers), and by keeping the characteristic impedance $Z_0$ as high as possible.

**Example 1**

The design specifications require to get IWS on an interconnection with:

- Threshold voltage $V_{TH} = 2.5 \text{ V}$,
- Characteristic impedance of the interconnection $Z_0 = 70 \ \Omega$,
- Open circuit output voltage from the driver in the High state: $V_A = 4 \text{ V}$

The designer can derive either the specification for the driver equivalent output resistance $R_O$, or the minimum value for driver output current $I_{OH}$.

The amplitude of the first incident wave (first step) can be evaluated from the open circuit output voltage, partitioned among the drive output resistance and the line impedance:

$$V_B = \frac{V_A \cdot Z_0}{Z_0 + R_O},$$

which solved in $R_O$ gives:

$$R_O = \frac{Z_0}{1} \left(\frac{V_A}{V_B} - 1\right),$$

$$R_O <= 42 \ \Omega$$

An alternate specification is the output current $I_{OH}$; the voltage $V_B$ can be written as:

$$V_B = Z_0 \cdot I_{OH}$$

To achieve IWS $V_B$ must be higher than the threshold voltage $V_{TH}$, that is:

$$I_{OH} = \frac{V_B}{Z_0},$$

$I_{OH} >= 35.7 \text{ mA}$

Effects of capacitive loading

The characteristic impedance $Z_0$ depends from the unit capacitance and inductance $C'$ and $L'$:

$$Z_0 = \frac{L'}{\sqrt{C'}}$$

When new receivers or transceivers are connected to the line (e.g. in backplane buses, as in figure 5.2), their input parasitic capacitance adds to the intrinsic line capacitance.

**Example 2**

A line with characteristic impedance $Z_0 = 70 \ \Omega$ has unloaded unit capacitance $C' = 50 \text{ pF/m}$ (no-load). We connect to the line 20 loads, 30 pF each (equivalent capacitance on a transceiver I/O pin) equally spaced over 50 cm.

Which is the new value $Z_0'$ of the line characteristic impedance ?

The distributed loads account for an additional unit capacitance $C'' = (30 \text{ pF x 20 loads}) / 0.5 \text{ m} = 1200 \text{ pF/m}$.

The reduction factor is $\frac{C'}{C' + C''} = 5$; therefore $Z_0' = 70/5 = 14 \ \Omega$.

The minimum value for driver output current $I_{OH}$ to achieve IWS (other parameters as in previous example) is now:

$$I_{OH} = \frac{V_B}{Z_0'},$$

$I_{OH} >= 178 \text{ mA}$

Such current is far higher than $I_{OH}$ of commercial logic devices.
Termination circuits

The current flowing in the termination resistance $R_T$ must come from (or go into) the driver. In the previous examples the termination resistance $R_T$ was always connected to ground. To drive a line with termination connected to ground at values higher than $V_{TH}$, the driver must have high $I_{OH}$. No current is required in the Low state.

If the termination resistance is tied to $V_{CC}$ (or to any voltage close to $V_{OH}$), no current flows in the high state and the current is about $V_{OL}/R_T$ for the low state. In this case the driver must have high $I_{OL}$.

For matched lines ($R_T = Z_0$) the current may rise to rather high values. For instance, with a termination $R_T = 70 \, \Omega$ and $V_{CC} = 5 \, V$ the output current $I_{OL} = V_{CC}/R_T = 70 \, mA$. This current flows into the driver, and adds to receiver input currents.

Due to asymmetry in the output stage, $I_{OL}$ is usually higher than $I_{OH}$, and therefore termination resistances are usually connected towards $V_{OH}$ rather than to ground. In the case of Open Collector drivers, the termination resistance acts also as pull-up resistance.

Several circuits can be used for terminations; some of them reduce the output current required from the drivers:

1. Passive termination

This termination is a simple pull-up towards $V_{CC}$ or a termination voltage $V_T$ (fig 5.3).

![Fig 5.3 Single-resistance termination.](image)

The voltage $V_T$ can come from a voltage divider or from a voltage regulator (fig 5.4).

![Fig 5.4 Termination to a voltage other than $V_{AL}$.](image)

If $V_T > V_{OH}$, the regulator must always supply a current. If $V_{OL} < V_T < V_{OH}$, the regulator must have current sink and source capability. Usual 3-term regulators (e.g. the 780x series) are not suitable in this last case; special regulators are available from the manufacturers.

2. Low power termination

The termination resistance is connected to signal ground though a capacitor, as in figure 5.5. On a voltage step, the capacitor acts as a short circuit, and the line is terminated by $R_T$. For steady line no current flows in the capacitor, and there is no static power consumption.

![Fig 5.5 Passive low-power termination.](image)

3. Active low power termination circuit.

The non-inverting buffer with positive feedback acts as a bistable circuit, which follows the state of the line (fig 5.6). On a state change, current flows in $R_T$ only as long as the output has not changed state yet. For a steady line no voltage difference appears on $R_T$, and no current flows.

![Fig 5.6 Active low-power termination.](image)

For any of these circuits, diodes connected to ground or to the power supply clamps spikes caused by reflected waves or by reactive devices (fig 5.7).

![Fig 5.7 Clamping the far end to block noise spikes.](image)
Driving point-to-point lines

This section describes the signals in transmission lines driven from one end. The first case discussed is a line open at the far end ($\Gamma_T = 1$) and matched at the driver ($R_O = Z_0$).

The first step in B ($t = 0$) has amplitude $V_A/2$ (partition of $V_A$ on $R_O$ and $Z_0$). At $t = t_P$ the first step reaches the far end (C), and is incremented by the reflected wave (with the same amplitude, since $\Gamma_T = 1$). The total step is twice the first step in B. At $2t_P$ the reflected wave comes back to the near end (B) and adds to the first step.

The system is now in its final state; there is no further reflection because the driver side of the line is matched. The waveforms are in figure 5.8 (where $1t_P$ corresponds to 2.5 horizontal divisions).

Fig 5.8 Near end (top trace) and far end waveforms for an open line with matched driver.

We will now analyze the same circuit as in previous example (line open at the far end: $\Gamma_T = 1$), with the driver no longer matched ($R_O < Z_0$, $\Gamma_G < 0$). Such mismatching occurs whenever we use high current drivers to get a high first step, because of their low equivalent output resistance.

Since $\Gamma_G < 0$, the signal reflected at the driver has opposite polarity with respect to original step. The steps on the line can be either positive or negative, with sign inversion every $2t_P$, (the time distance between reflections at driver).

At the far end C, where incident and reflected wave sum with the same polarity, the actual waveform can oscillate. These oscillations may bring the voltage to cross several times the logic threshold $V_{TH}$, thus causing additional logic state changes.

Fig 5.9 Near end (top trace) and far end waveforms for an open line with high-current, low-resistance driver.

To avoid unwanted logic state changes caused by high current drivers we could match the line at the far end. This parallel termination is a load, and increases static power consumption.

Another possibility to block oscillations is to match the line at the driver side, with a resistance $R_G$ connected between the line and the driver output, as in figure 5.10. If $R_G + R_O = Z_0$, the total equivalent resistance at the driver side is $R_O' = Z_0$, and the backward wave (travelling from C to B) is fully absorbed at the driver.

Fig 5.10 Series termination.

At the driver side we can observe a double step (incident wave at $t=0$, reflected wave at $t = 2t_P$) on the open end we get a single step with double size (incident plus reflected wave) at $t = t_P$ (Figure 5.11).

This technique is called *series termination*, and is widely used to drive address and control lines of small memory banks. It uses less power then parallel termination at the far end, but can be used only for point-to-point interconnections, driven from one end.
Driving bused lines

A driver connected to an intermediate point E of a uniform line with characteristic impedance $Z_0$ is loaded by an impedance $Z_0/2$ (Fig 5.12). To get incident wave switching, the driver output impedance must be very low (that is, the driver must be able to source or sink a high current). In the node E we have three parallel branches, respectively with impedance $Z_0$, $Z_0$, and $R_O$. The equivalent impedance in E is always less that $Z_0$, and the corresponding reflection coefficient $\Gamma < 0$. The polarity of reflected waves is inverted and the voltage on the line can oscillate as in the previous example.

Since another branch of line is connected at driver output, source termination in the node E is not possible ($Z_0$ in parallel to any other impedance is always less than $Z_0$). To absorb the reflections it is necessary to terminate the line at both ends. This is the typical case of multipoint buses (for instance backplane buses, where several boards can be connected at many positions).

In multi-point buses, many devices (active driver, receiver, disabled drivers, and passive loads) are tied to each line. The capacitive load lowers the propagation speed and the characteristic impedance of the line (a 100 $\Omega$ line can go below 20 $\Omega$ due to additional capacitance; the propagation speed scales the same factor). Driving low impedance lines requires high-current devices, and high current means more heat to dissipate and more noise towards other circuits (that is a EMC problem). Therefore it is mandatory design practice to limit the capacitive load on each line.

The board must use a single transceiver towards the bus (figure 5.13, left). The transceiver isolates all on-board circuits and reduces the capacitive loading on bus lines. Direct connection of on-board devices to bus lines (figure 5.13, right) must be avoided, since it increases the capacitive load and lower the characteristic impedance.
Design guidelines

High-speed logic systems must use multiple layer Printed Circuit Boards (PCB), with alternated signal layer and ground/supply layers, to provide a controlled environment for signal propagation. Example of signal track layers and ground plane are in figure 5.15.

Fig 5.15 Tracks and ground plane in a PCB.

In summary, to get high transfer speed and reliability in a multipoint bus connection we must:
- limit capacitive loading by inserting isolation buffers on each board;
- place drivers and receivers as close as possible to the bus connector;
- choose small packages, with low parasitics;
- use multilayer PCB, to get a well defined transmission line environment.

Review questions

1) The correct value of a series termination resistance $R_S$ is:
- $R_S = Z_0 + R_O$  
- $R_S = R_O - R_T$
- $R_S = Z_0 - R_T$  
- $R_S = Z_0 - R_O$

The sum of driver output resistance and external series termination must equal the line characteristic impedance.

2) To avoid reflections with mid-point driving bused lines, one has to:
- leave line ends open,
- put series termination on all drivers,
- place matched parallel termination at both ends,
- place matched parallel termination at one end only.

Since three branches (two transmission lines and the driver output) converge at the driving node, it is not possible to match the line at the driver side. The only possibility is to avoid reflections at the far ends, by matched terminations.

3) In a mid-point driven 100 ohm bused line, the amplitude of the first step, for $V_A = 5 \, \text{V}$, $R_O = 50 \, \Omega$, is:
- 1 V,  
- 1,25 V,  
- 2,5 V,  
- 5 V.

The driver sees a $Z_0 / 2$ load ($Z_0 / Z_0$). Use of the equation: $V_B = V_A \times Z_0 / (Z_0 + R_O)$ gives:

$$V_B = 5 \times 50 \, \Omega / (50 + 50 \, \Omega)$$

4) A 20 cm PCB track with unit capacitance 30 pF/m is loaded with 10 loads with equivalent capacitance 10 pF, evenly spaced. The unloaded line impedance is 150 $\Omega$. The approximated loaded line impedance is:
- 200 $\Omega$,  
- 100 $\Omega$,  
- 10 $\Omega$,  
- 35 $\Omega$.

The loaded line impedance can be calculated as: $Z'_0 = \sqrt{\frac{L}{C}}$; since the unloaded impedance is $Z_0 = \sqrt{\frac{L}{C}}$, the impedance reduction factor is $1 - \frac{C' + C''}{C}$.

The added unit capacitance is $C'' = (10 \times 10 \, \text{pF}) / 20 \, \text{cm} 	imes 100 \, \text{cm} = 500 \, \text{pF/m}$.

$$\sqrt{\frac{C' + C''}{C}} = \sqrt{\frac{30 + 500}{30}} = \sqrt{17.66} = 4.2$$

Loaded line impedance $Z' = 150/4.2 = 35.68 \, \Omega$. 