Interconnections for high-speed digital circuits

Signal Integrity in Digital Circuits

Lesson 1: Crosstalk

Goal

The exchange of information in an electronic system can be compromised by signal degradation and by disturbances generated either outside or inside the systems itself. The signal integrity addresses these problems: it enables the designer to guarantee correct signaling within a system, taking into account the physical laws of electrical signal propagation, and in spite of disturbance and noise originated within the system itself.

Current high-speed digital systems require designers able to think not only in terms of "0" and "1" (standard Boolean algebra), but also in terms of current, mutual inductance, transmission lines, parasitic parameters. Signal integrity involves skills from digital and analog electronics, and electromagnetic wave propagation theory and practice. An understanding of these problems is now mandatory for any digital system designer.

After this course you will know what "Signal Integrity" means and how to deal with these problems in high speed digital systems, by using proper design techniques, by proper selection of the logic family, and applying some PCB layout design rules.

Content and organization

The Signal Integrity in Digital Circuits course is structured in 5 lessons:

- Crosstalk
  - Capacitive and inductive coupling, Crosstalk Model, Forward and Backward crosstalk.
  - Design Guide to reduce Crosstalk.
- Ground bounce and switching noise
  - Effects of PCB layout. Signal and ground routing. Filtering
- Design guide for Ground and Power planes.
  - Ground bounce, simultaneous switching noise, totem-pole current spike.
  - Decoupling Capacitors, PCB layers stacking. Ground and power distribution. Clock distribution

Prerequisites

To follow these lessons you must already know
- circuit theory: R-C cells, transient response,
- loss-less transmission lines,
- structure of digital logic circuits, static parameters
- dynamic interfacing of digital circuits
- function and use of basic electronic instruments (pulse generator, oscilloscope).
References

A reference textbook with both general and detailed discussion of signal integrity problems is:

H.W. Johnson, M.Graham: 
High Speed Digital Design (A Handbook of Black Magic), 

The same author has a web site, with several articles and pointers:

http://www.signalintegrity.com/ftrecord.htm

Other more specific references are provided in each lesson.

Other textbooks with general references on this subject are:

M.I. Montrose:
PCB Design Techniques for EMC Compliance, 

Henry W. Ott
Noise Reduction Techniques in Electronic Systems
John Wiley&Sons, 1988

James E. Buchanan
Signal and Power Integrity in Digital Systems: TTL, CMOS and BiCMOS
McGraw-Hill, 1996

For this lesson, the related sections in the reference book are: 3.9 and 5.7.

Acknowledgements

The photographs have been taken by the author during the laboratory exercises of courses held at the Politecnico di Torino. Some of the drawings are screen captures from simulators developed by the author or for the “Elettronica II” course CD-ROM developed by COREP, and from the “Electromagnetic Compatibility CD-ROM developed within the CAMPUS-CRUI project.

Summary

Conductors running side-by-side (e.g. bus tracks) exhibit capacitive and inductive coupling. Due to these coupling, a signal driven on one line can induce noise on the other ones; this behavior is called crosstalk.

The first lesson answers to the following questions:

- What does “signal integrity” mean ?
- Which are typical signal integrity problems
- Which are the effects of mutual coupling among PCB conductors ?
- How can mutual coupling cause false signaling ?

Examples of signal integrity problems

1) In a bundle of wires only some of them are active (that is carry logic transitions), but signals appear also on not-active conductors. This is a crosstalk problem, and can be handled by proper selection of driving devices and wiring layout.

Fig 1.1 Crosstalk from capacitive and inductive coupling.

2) A pulse is applied to one input of a buffer; the other inputs of the same package are fixed at High or Low levels. The voltage at the outputs corresponding to steady inputs change state when other devices in the same package switch. This can be caused by ground bounce noise – a common-path crosstalk problem - and can be avoided by proper layout and decoupling of the power supply.

Fig 1.2 Crosstalk caused by ground bounce.

Simplified Model for Crosstalk Analysis
The reference model for a first approximation analysis of crosstalk consists of two wires (or PCB tracks) running close each other, as in figure 1.3.

**Fig 1.3 Two coupled tracks.**

For this analysis the wires are modeled as two transmission lines with characteristic impedance $Z_0$ and both capacitive ($C_M$) and inductive ($L_M$) coupling. To avoid multiple reflections, both lines a have matched terminations $R_T = Z_0$. (figure 1.4).

**Fig 1.4 Transmission line model for crosstalk analysis.**

The driven line (or active line, always drawn in the upper part of the diagram) carries a signal moving at speed $U$. This signal is a voltage step with rise time $t_r$ and slope $\frac{\Delta V}{t_r} = \frac{\Delta V}{t_r}$. (Figure 1.5).

**Fig. 1.5 Disturbing signal.**

The effects of capacitive coupling can be evaluated with the model shown in figure 1.6. The equivalent circuit includes a voltage generator $V_{SC}$, the coupling capacitance $C_M$, and the impedance $Z_0/2$, which models the resting (or passive) line.

**Fig 1.6 Model for capacitive crosstalk**

If the voltage change $V_{SC}$ on the passive line is small, the whole step $V_S$ appears through the capacitor $C_M$. A current $I_{CM} = C_M \frac{\Delta V}{t_r}$ flows from the capacitor to the load $Z_0/2$. This rectangular current pulse generates a voltage pulse with the same duration $t_r$ and amplitude $V_{SC} = I_{CM} \frac{Z_0}{2}$. In summary:

$$V_{SC} = I_{CM} \frac{Z_0}{2} = C_M \frac{\Delta V}{t_r} \frac{Z_0}{2} = C_M \frac{\Delta V}{l_s} \frac{Z_0}{2}$$

This pulse propagates on the passive line towards the two ends of the passive line, thus making the Backward Capacitive ($B_C$) and Forward Capacitive ($F_C$) terms of crosstalk (figure 1.7).

**Fig 1.7 Forward and backward propagation of the capacitive term**

The inductive coupling causes on the passive line a voltage proportional to the concatenated magnetic flow change, and therefore again to $\frac{\Delta V}{t_r}$. The induced voltage is $V_{SL} = L_M \frac{\Delta V}{t_r}$. (Figure 1.8).

**Fig 1.8 Model for inductive crosstalk**

Also this voltage propagates on the passive line towards the two ends with opposite polarity in the two directions: Backward Inductive ($B_L$) and Forward Inductive ($F_L$) terms of crosstalk (figure 1.8). In this case, since the induced disturbance can be modeled by a voltage generator serially connected along the passive line, the backward and forward pulses have opposite polarity.
Forward and backward crosstalk

In summary, the disturbing signal propagating on the active line puts on the passive line four noise signals or crosstalk terms, all with amplitude proportional to $\frac{dv}{dt}$ and duration $t_r$:

1. crosstalk caused by coupling through $C_{M}$, which propagates towards the termination (right side):
   - Forward Capacitive crosstalk $F_{C}$

2. crosstalk caused by coupling through $C_{M}$, which propagates towards the driver (left side):
   - Backward Capacitive crosstalk $B_{C}$

3. crosstalk caused by coupling through $L_{M}$, which propagates towards the termination (right side):
   - Forward Inductive crosstalk $F_{L}$

4. Crosstalk caused by coupling through $L_{M}$, which propagates towards the driver (left side):
   - Backward Inductive crosstalk $B_{L}$

The total crosstalk moving towards the right end (far end, termination), in the same direction of the disturbing signal is the forward crosstalk $F_T = F_C + F_L$. Forward crosstalk is the sum of terms 1 and 3 above; since they have the same polarity, if $\frac{dv}{dt} > 0$ (for the disturbing signal), the forward crosstalk is always positive.

The total crosstalk moving towards the left end (near end, driver), in the opposite direction of the disturbing signal is the backward crosstalk $B_T = B_C + B_L$. Backward crosstalk is the sum of terms 2 and 4 above; since they have opposite polarity; the actual polarity of backward crosstalk depends on prevalence of capacitive (2) or inductive (4) term.

The above mentioned disturbance are generated on each elementary section of line: the actual voltage $v(x,t)$ at any point of the line is the sum of all these contributions. The disturbing pulse moves towards the far end with speed $U$, and the forward term moves in the same direction at the same speed. At any point along the line all the forward terms previously generated arrive at the same time, and sum up to make a single pulse of width $t_r$ and increasing amplitude as it moves along the line towards the far end. The forward term at different points along the line is visualized in figure 1.10. These are the signals which can be observed on a scope connected to the resting line, when an edge travels along the disturbing line.

When the disturbing edge reaches the far end at $t = t_P$, it is absorbed by the matched termination, and the corresponding noise generators turn off. The forward term ends immediately; the various points along the line return to the resting voltage as the "turn off" propagates backwards towards the driver.
Examples

The following drawings are taken from an algorithmic simulator, which separates the waveforms of forward and backward crosstalk components for different capacitive and inductive coupling. This split is not possible in a real systems, where the voltage in any point of the line is the sum of forward and backward waves. The three diagrams are snapshots of the voltage on the disturbing line (upper diagram), and of forward and backward terms on the resting line (respectively second and third diagram from the top). Note that these diagrams represent v(x) at a given t; they are not v(t) diagrams taken at given points on the line, like the scope diagrams in figure 1.10 and 1.11. The waveforms are idealized (rectangular pulses); in real systems edges are rounded, and rise/fall times of crosstalk signals are not zero.

The first diagram (Fig 1.12) shows the crosstalk voltages at t = tP/3, for a given combination of dV/dt (rise time tr of the disturbing edge), CM , and LM  (the values of these parameters shown in the box at the bottom right corner are only for comparison of different situations).

Fig 1.12 Crosstalk noise at t = tP/3.

Figure 1.13 shows the same waveforms for the same system at a later time t = 2 tP/3 . The forward term amplitude increases (due to summation of contributions along the line), but the duration is still tr, while the backward term keeps the same amplitude but longer duration.

Fig 1.13 Crosstalk noise at t = 2 tP/3.

In the third diagram (Fig. 1.14), the ratio among capacitive and inductive coupling is inverted: the capacitive term overcomes the inductive one, and the polarity of resulting forward term is reversed.

Fig 1.14.. Crosstalk noise at t = tP/3, with higher capacitive coupling.

The effects of edge slope are shown in figure 1.15. All parameters are the same in both cases, the only difference being the slope of the disturbing signal rising edge. Since crosstalk amplitude is proportional to the slew rate, the steep edge causes a higher noise. The disturbance lasts for the duration of the edge, and is close to 0 when the active line does not change state.

Fig. 1.15 Crosstalk pulses for steep and slow edges.
Near-end and Far-end crosstalk

The actual cross talk signals in a real system are the sum of all contributions (inductive, capacitive, forward and backward terms). Due to different propagation directions, the waveforms depend on the observation point: a scope connected to different points shows different wave shapes. Summarizing the previous analysis:

At the near end all terms start for \( t = 0 \); the backward term ends when the disturbing pulse reaches the far end, and the induced noise generator is turned off (at \( t = t_p \)). This information (or the negative edge caused by turning off the disturbing pulse at the far end) needs another \( t_p \) to reach the near end, therefore the total duration of crosstalk noise at the near end is \( 2t_p \) (track A in figure 1.16).

The disturbing pulse (and induced noise) reaches the far end at \( t = 2t_p \) (nothing can be seen before). The forward term (narrow pulse with width \( t_r \)) is the sum of all contributions along the line; the backward term ends almost immediately, as the disturbing pulse reaches the far end at the same time end at \( t = 2t_p \). Therefore the far-end crosstalk is a narrow pulse, occurring at \( t = 2t_p \), with sign and amplitude related with the actual \( L_x \) and \( C_y \) values (track C in figure 1.15). At intermediate position (track B in figure 1.16) we can observe the forward term (narrow pulse, variable height), followed by the backward term (rather flat pulse, width depending on the position).

Fig. 1.16 Measurement of total crosstalk.

Review questions

1) A processing system suffers intermittent failures; the error rate changes (but never goes to 0) when the power supply voltage changes of a few %, some IC are replaced, or interface boards are moved to other slots. The correct countermeasure is:

- rewrite the program in another language,
- analyze the OS interfaces,
- *revise the electrical design, focusing on dynamic interfacing and signal integrity aspects,
- put a voltage regulator on the power supply.

These symptoms reveal random errors, which cannot depend from the SW (repeating the operations with the same data should give identical results), nor from the power supply. Too narrow electrical interfacing margins make the system sensitive to noise and disturbance, which cause small changes in signal levels and power supply voltage.

2) The term which best describe the problem addressed by signal integrity is

- static compatibility of logic circuits
- power consumption of logic circuits
- *dynamic behavior of logic signals and circuits
- correctness of Boolean operations performed by logic gates

Static compatibility is also a condition to fulfill, but the correctness of dynamic behavior requires also static compatibility.

3) The amplitude of crosstalk noise is

- *proportional to the slew rate (\( dV/dT \)) of the disturbing signal
- inversely proportional to the slew rate (\( dV/dT \)) of the disturbing signal
- not affected by the slew rate of the disturbing signal
- proportional to the duration of the disturbing signal

The crosstalk is directly proportional to mutual coupling (capacitive and inductive) and on slew rate of signals. Steep edge, with fast slew rate push more noise through capacitive and inductive coupling.

4) The backward crosstalk noise term at the near end has:

- fixed amplitude, duration \( t_r \)
- amplitude proportional to line length, duration fixed
- amplitude and duration proportional to line length,

The backward term can be seen as the sum of all contributions along the line, originated when the disturbing pulse travels towards the far end. When the pulse reaches the far end (for a matched line), it is absorbed by the termination. The backward pulse duration is therefore twice the propagation time, which in turn depends from line length.
5) The forward crosstalk noise at the far end has:
- fixed amplitude, duration $t_r$,
- fixed amplitude, duration proportional to line length,
- *amplitude proportional to line length, fixed duration,
- amplitude and duration proportional to line length.

The forward term can be seen as the sum of all contributions along the line, originated when the disturbing pulse travels towards the far end. Since these elementary contribution travel towards the far end at the same speed of the disturbing pulse, their amplitude increases as the signal moves toward the far end. The final peak value is therefore proportional to the length of the line.

6) At the near end we can observe a crosstalk noise pulse with duration
- $t_r$, $2t_r$, $t_P$, $2t_P$.

The total width of the near end crosstalk pulse depend from the time required by the disturbing signal edge to travel along the line ($t_P$), plus the time require by the negative edge (the crosstalk noise turn-off) to come back to the near end (another $t_P$).

7) At the far end we can observe a crosstalk noise pulse with duration
- $t_r$, $2t_r$, $t_P$, $2t_P$.

The far end crosstalk pulse is the sum of all elementary contributions along the line, which move towards the far end at the same speed of the disturbing signal. They sum in the amplitude domain, and the pulse width corresponds to the width of each elementary contribution ($t_r$).

8) If the characteristic impedance $Z_0$ of the disturbed line increases, the capacitive term of crosstalk:
- does not change, increases, decreases.

The amount of capacitive crosstalk depends on the partition among the mutual capacitance $C_M$ and the line characteristic impedance $Z_0$. As $Z_0$ goes up the attenuation decreases, and the noise transferred through capacitive coupling to the resting line increases.

9) Connecting a scope at the middle point of the disturbed line we will observe:
- a pulse with duration $t_r$ followed by a spike of duration $t_r$, 
- a pulse with duration $2t_r$ followed by a spike of duration $t_r$, 
- *a spike of duration $t_r$ followed by a pulse with duration $t_r$, 
- a spike of duration $2t_r$ followed by a pulse with duration $2t_r$.

The signal at any point is the sum of the forward term (a spike of duration $t_r$) and the backward term (a pulse with duration twice the fly time from that point to the far end, that is $t_P$ for the line middle point).

10) If the length of a couple of lines is doubled (and all other parameters per unit length remain unaffected):
- the amplitude of near-end crosstalk doubles, 
- *the amplitude of far-end crosstalk doubles, 
- the width of far-end crosstalk doubles, 
- the amplitude and the width of near-end crosstalk doubles.

The far end crosstalk pulse is the sum of all elementary contributions along the line, which move towards the far end at the same speed of the disturbing signal. Therefore the amplitude of far end crosstalk is proportional to the line length.
Signal Integrity in Digital Circuits

Lesson 2: Design guide to handle crosstalk

Summary

The physical laws that causes crosstalk cannot be modified, but proper design can keep under control both the amount of crosstalk (passive countermeasures), and its effects (active countermeasures). This lesson presents the design technique for electronic systems which allow to reduce the errors originated by crosstalk.

More in detail, the following questions can be answered by this lesson:

- Which are the actual effects of crosstalk?
- How can the designer keep under control these effects?
- What does “active countermeasures” mean, and how can be put to work?
- Which are the “passive countermeasure” at the circuit and system level?

References

For this lesson, the related sections in the reference book are: 9.1, 9.2, 9.3, 10.1, 10.2, 3.9, and 5.7.

Effects of crosstalk

The previous lesson described how mutual coupling can induce noise pulses on conductors which should stay in a fixed logic state. These pulses have amplitude and width related with the characteristics of the disturbing signals and the electrical parameters of the system. For instance, the capacitive term can be evaluated as:

\[ V_{SC} = \frac{Z_{D}}{2} \cdot \frac{\Delta V}{t} \cdot Z_{0} \]

and the inductive term:

\[ V_{SL} = L_{M} \cdot \frac{\Delta I}{t} \cdot Z_{0} \]

If these voltages and currents cross the logic threshold of logic devices, they may be interpreted as false logic states. The goal of the designer is to avoid errors caused by these spurious logic states, and can be achieved through a series of countermeasures:

Passive countermeasures limit the amount of crosstalk noise, by controlling the parameters of the signals and of the physical system.

Active countermeasures limit the effects of noise towards logic circuits (the spurious pulses, even if present, is not translated into a false logic state). These techniques exploit some characteristics of noise signals, such as the limited duration or energy. The top level active countermeasure include error correction techniques, which can mask errors at the electrical level, and are not addressed here.

Passive countermeasures

Both the capacitive and the inductive terms are proportional to the disturbing signal slew rate \( \frac{\Delta V}{t} \), or, for a simplified triangular wave \( \frac{\Delta V}{t} \).

Reducing \( \frac{\Delta V}{t} \) means to use low-voltage logic devices (which provide benefits also for power consumption and external EMI). Unfortunately a simple voltage scaling affects also the logic threshold: if we reduce the voltage difference among the HIGH and LOW logic states, the noise margin is proportionally reduced, and lower noise pulses can still cause false signaling. To keep the noise margin we must use devices with tight control of threshold; these are discussed in the active countermeasure section.

Increasing \( t \) means to use low-speed logic circuits (the slowest logic family which allows to fulfill timing specifications). The slow transition among logic states may cause other problems (e.g. long totem-pole current pulses – see lesson 3). A first fundamental design rule is:

Use the slowest logic family compatible with speed requirements of the system.

Controlled slope drivers have been designed for best performance in driving long lines. These devices keep \( \frac{dv}{dt} \) under control even in fast switching circuits. The output stage consists of several transistors which are turned on in sequence. The total equivalent resistance is low, but the current is kept to limited value (at the expense of an increase in the switching time).
The other key parameters are the capacitive and inductive coupling. All printed circuit boards (PCBs) and cables exhibit capacitive coupling among tracks or conductors, a proper use of screens and ground conductors may substantially reduce these parasitic capacitance. Mutual capacitance in printed circuit boards depends on distance among tracks and from adjacent grounds. Ground tracks and ground planes add capacitance between signal tracks and grounds, but reduce mutual track-to-track capacitance.

- **internal ground layer**: cuts capacitive coupling between tracks on external sides (Figure 2.3);
- **alternating signal-ground tracks**: cuts capacitive coupling between adjacent tracks (Figure 2.4);
- **ground-signal-ground sandwich**: the characteristic impedance is precisely defined, and couplings are minimized (Figure 2.5).

The qualitative effects are summarized in the following table:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Characteristic Impedance</th>
<th>Crosstalk</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB track without ground plane</td>
<td>200 ohm</td>
<td>50%</td>
</tr>
<tr>
<td>PCB track with one ground plane</td>
<td>80 ohm</td>
<td>25%</td>
</tr>
<tr>
<td>PCB track with ground plane on both sides</td>
<td>100 ohm</td>
<td>11%</td>
</tr>
</tbody>
</table>

A second fundamental rule, for PCB and interconnection systems (cables) designers is:

**Reduce capacitive coupling by separating wire/tracks and by using screens (ground layers, ground tracks);**

Inductive coupling is more difficult to visualize than mutual capacitance: there is no real “magnetic screen”, but the designer can manage to avoid transformer-like structures, which exhibit high mutual inductance.

In digital systems signal and ground return make loops, as in figure 2.6.

Ground currents follow the lowest impedance path, that is the minimum resistance for DC or low frequency, and minimum inductance path for high frequency components. The inductance is proportional to the concatenated magnetic flow of a wire loop, which depends on the loop area. Therefore to keep inductance low we must minimize loop area by providing a return path as close as possible to the signal conductor.
When the PCB has a continuous ground plane, the return current follows a minimum impedance path with minimum loop area, that is as close as possible to the signal conductor, as in figure 2.7a.

In the ground plane of a multilayer PCB, holes are used to create conducting vias among different layers. A group of adjacent holes makes a slot. Holes and slots break the ground plane and force currents to form more wide loops (for this aspect slots are worse than holes). Return paths looping around a slot is shown in figure 2.7b.

Fig 2.7 Photo of the ground plane is a multilayer PCB. The yellow line corresponds to the signal track (on another layer).

a) The green return path can travel on the ground plane without forming loops  
b) The return path must loop around a slot.

On connectors and flat cables, special care must be taken in positioning ground pins and wires. If the return current flows far from corresponding signal the path makes wide loops.

Fig 2.8 A wide loop can be made thinner by moving the GND pin near the signal pin.

If the loops made by signals and ground returns have significant shared area, they make a transformer (with single-turn windings in air): with high mutual inductive coupling. If the loops have no common area: the inductive coupling is minimized (figure 2.9).

Fig 2.9 Two nested loops can be decoupled using independent GND pins for each signal.

Flat cables, with several conductors running at close spacing for some distance, may have strong inductive coupling. Independent ground returns on pins close to signals, minimizes the inductive coupling, while using the same pin for return currents from several signals creates nested loops with high mutual inductance, as shown in figure 2.10.

Fig 2.10 Signal (Si) – Ground loops in a flat cable. The numbers of GND connections is the same in both cases, but b) exhibits far less inductive coupling.
A similar problem occurs with arrays of termination resistor: devices with a common VT pin shared by many termination resistances have mutual coupling higher than independent-resistors arrays.

![Fig 2.11a) termination array with common VT pin: high inductive coupling, b) independent resistors termination array: low inductive coupling.](image)

A second fundamental design rule for designers is therefore:

**Reduce loop areas by providing return paths as close as possible to signal paths,**

and

**Reduce inductive coupling by avoiding nested loops.**

### Active Control of Crosstalk

Controlling the slope of signal edges is a passive countermeasure, which reduces the amount of generated noise. The same technique can be used to blocks short spikes. A dV/dt limiter (a logic buffer with controlled slope) in the signal path can filter short noise pulses.

![Fig 2.12 Effect of a slew rate limiter.](image)

Both the inductive and the capacitive terms of crosstalk have a duration shorter than 2 tₚ; if the logic circuits is not sensitive to logic state changes with duration shorter than 2 tₚ, crosstalk pulse – even if present - are blocked before entering the logic devices. This time-filtering function is accomplished by integrating receivers.

The block diagram of an Integrating Receiver is in figure 2.12:

![Fig 2.13 Comparison between standard logic and Enhanced Transceiver Logic.](image)
**Review questions**

1) **Signals with limited slew rate allow to**
   - reduce inductive crosstalk only,
   - reduce capacitive crosstalk only,
   - reduce capacitive AND inductive crosstalk, has no effect on crosstalk.

Both inductive and capacitive crosstalk are proportional to the disturbing signal slew rate.

2) **Which of the following countermeasures has NO EFFECT on capacitive crosstalk**
   - use of ground planes,
   - guard tracks between signal tracks, connected to ground at one end,
   - use separate grounds for each signal,
   - avoid nested signal-ground loops.

Using separate grounds reduces the nested current loops. This reduces mutual inductive coupling, but has no effect on capacitive coupling.

3) **Which of the following countermeasures has NO EFFECT on inductive crosstalk**
   - use of ground planes,
   - guard tracks between signal tracks, connected to ground at one end,
   - use separate ground for each signal,
   - avoid nested signal-ground loops.

Guard tracks act as electrostatic screen, and reduce mutual capacitance. They could reduce also inductive coupling if used as individual return paths for signal currents.

4) **Which is the most effective passive countermeasure to reduce capacitive crosstalk**
   - PCB with internal ground layer
   - alternating signal-ground tracks
   - alternating signal-ground tracks, and ground-signal-ground layer sandwich

The ground tracks interleaved between signal tracks and the ground layers above and below the track are a good approximation of a complete screen around the signal conductor.

5) **Which logic family is the best choice to limit the crosstalk ?**
   - the fastest commercially available within cost budget limits,
   - the slowest compatible with timing specifications,
   - the latest one, independently from speed and cost,
   - the family which uses less static power.

Using slow logic families keeps the dV/dt of signal edges; the noise towards other parts of the system is proportional to disturbing signal slew rate. However, the circuit speed must comply with timing requirements (system-operation is a requirement as mandatory as low crosstalk).

6) **Integrating receivers**
   - block capacitive crosstalk only,
   - block inductive crosstalk only,
   - filter any pulse shorter than a predefined time,
   - block any pulse longer than a predefined time.

The integrating receiver is a time-domain filter, which allows logic state changes to go through only if they last longer than the time threshold of the receiver. Short pulses are ignored, independently of their origin.

7) **Which of the following layouts is more effective to reduce inductive coupling in a flat cable (G = Gound wire, S = Signal wire):**
   - S G G S G S G S, G S G S G S G S
   - G G S S S S G G, S S S S G G G G.

Alternating signal and ground wires minimizes the common area of the loops, thus reducing mutual inductive coupling.

8) **Slots in ground planes**
   - increase mutual inductive coupling,
   - decrease mutual inductive coupling,
   - increase mutual capacitive coupling,
   - decrease mutual capacitive coupling.

Inductive coupling comes from nested signal-return current loops. A continuous ground plane allows return current to circulate as close as possible to the signal track, thus minimizing the loop area. A slot in the ground plane may force the current to run on a path longer and away from the signal, thus increasing connection inductance and coupling with other circuits.

9) **A sequence of two integrating receiver with time thresholds \( T_f \) (each)**
   - block pulses shorter than \( T_f \),
   - block pulses shorter than \( 2T_f \),
   - block pulses longer than \( T_f \),
   - does not block any pulse.

Signals longer than the time threshold are delayed by an integrating receiver, not modified in any other manner. Therefore the combined effect of a sequence of integrating receivers is filtering with the shortest time threshold, and delaying the sum of individual delays.
Signal Integrity in Digital Circuits

Lesson 3: Ground bounce and switching noise

Summary

The previous lessons presented spurious signaling originating from capacitive and inductive coupling among interconnecting wires or parts of the interconnection, such as connectors and termination resistances. There are also other sources of noise within the system: when ground and supply paths are shared among different devices, the voltage drop caused by the ground currents of a device may affect the behavior of other devices. This is the common path crosstalk, which causes simultaneous switching noise and ground bounce, described in this lesson.

This lesson answers to the following questions:
- How can common paths cause crosstalk?
- Which are the causes of ground bounce?
- Which is the relation between simultaneous switching and ground-bounce?
- Why ground-bounce is a type of crosstalk?

References

For this lesson, the related section in the reference book is 5.1.

The totem-pole Current Spike

The output stage of logic circuits is made with two active devices (transistors), which act as switches with complementary commands. In first approximation, the equivalent circuit of a logic output is a SPDT (Single Pole Double Throw) switch, as shown in figure 3.1. (the diagrams show CMOS device, but similar consideration apply also to bipolar logic circuits).

With such circuit no current can flow from the power supply VDD to GND - this is the reason for the 0 steady state power consumption of CMOS circuits. A more accurate analysis must take into account the analog behavior of the transistors: they toggle among the ON and the OFF states in a soft manner, and go into intermediate states during the logic transitions. When both transistors are in light conduction a current $i_S$ flows directly from $V_{DD}$ to GND, as shown in figure 3.2.

Wire bond and Flip-chip have far lower parasitic inductance due to shorter connections

<table>
<thead>
<tr>
<th>Package</th>
<th>Inductance on each pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP 14</td>
<td>10 nH</td>
</tr>
<tr>
<td>DIP 68</td>
<td>100 nH</td>
</tr>
<tr>
<td>PLCC</td>
<td>10 nH</td>
</tr>
<tr>
<td>Wire bond</td>
<td>1 nH</td>
</tr>
<tr>
<td>Flip chip</td>
<td>0.1 nH</td>
</tr>
</tbody>
</table>

Fig 3.1 – Simplified model of a logic output.

Fig 3.2 – Current flow during logic transition (Totem Pole current spike).

The duration of the current pulse depend on the speed of the input transition; if it is too slow (e.g. if the input is indefinitely kept near $V_{TH}$), the current flow may damage the device due to overheating. Since only totem-pole outputs exhibit this behavior (Open Collector have only one active device towards GND), this current is called Totem Pole Current Spike.
The current spike at state change is far higher than DC current in steady state, and it causes voltage drops due to the impedance of the ground and power connections. The shift in the ground voltage is:

$$V_G = L_G \frac{\Delta i}{\Delta t} \quad \text{or} \quad V_G = R_A \frac{\Delta i}{\Delta t}$$

where $\Delta i$ is the rise time of the current. A similar drop occurs on the power supply lead (inductance $L_S$). The actual supply voltage at the device pin is $V_{ALE} = V_{AL} - V_S - V_G$.

These voltages become noise on all other nodes (outputs and inputs) in the same package, and modify both the actual input voltage (thus causing possible false transitions), and the outputs which should stay in a steady state.

The shift in ground potential due to switching noise affects all nodes of the device, and may cause false signaling. It is referred to as ground bounce.

Current flow in the output capacitance

To change the voltage level $V_{OUT}$ at the output node, the output stage of the logic gate must charge or discharge the capacitance $C_O$ associated to that node. This again means a current flow through the output stage from $V_{DD}$ (L-H transitions, figure 3.3) or towards GND (L-H transitions, figure 3.4).

The following values can be used for a first rough evaluation of the actual total capacitance:

- Logic inputs: 2-10 pF
- Logic outputs: 20-50 pF

Since a significant part of this capacitance comes from the package, smaller packages have lower capacitance.

Total Ground bounce

The current flowing in the output of a driver comes through the power and ground pins. The totem pole spike and the output capacitance charge current occur at any output node, and the total current depends on the number of simultaneously switching outputs. When many drivers are included in the same package, the currents for each output must flow through the device power and ground pin. With severe capacitive loading (such as in buses, where many input or disabled 3-S outputs are connected to each line) the current spike at state change can go to rather high levels.
Numerical example 1:
A logic output drives 10 loads, with equivalent input capacitance of 30 pF each (typical value of equivalent output capacitance for a disabled 3-S output)

The total capacitance is $C_T = 300$ pF

$V_{OL} = 0.5$ V and $V_{OH} = 4.5$ V (typical values for CMOS logic)

The voltage change among logic states is 4 V; assuming a rise time $t_f$ of 4 ns, the current can be evaluated from the relation:

$$i = \frac{C}{t_f} \Delta V$$

$$i = \frac{300 \text{ pF} \times 4 \text{ V}}{4 \text{ ns}} = 300 \text{ mA}$$

(current for a single driver, assuming constant slew rate voltage at the output)

The current spike caused by charge and discharge of the output capacitance may cause voltage drops due to the impedance of the ground and power connections, which can be evaluated as

$$V_G = L_G \frac{\delta i}{\delta t} \quad \text{or} \quad V_G = L_G \frac{\delta I}{\delta t}$$

In the previous example, under the assumption of triangular voltage and rectangular current, the current slew rate should be infinite, therefore we need a better model, as shown in figure 3.6.

Fig 3.6 Linear model (a) and real waveforms (b).

We can analyze the ground bounce for a HIGH-LOW transition, using these simplified models for current and voltage waveforms.

The (equivalent) load capacitor $C_L$ is charged at $V_H$ and, during the state transition, is discharged to $V_L$. We assume an "ideal" driver, with $R_O = 0$, but will take into account the inductance $L_G$ of the interconnection from the drain of the output transistor (lower node of the switch in our model) to the system ground reference. $C_L$ is directly connected to the reference ground. The output step from $V_H$ to $V_L$ is a rounded trapezoidal waveform.

The current in the capacitor is the derivative of the voltage:

$$i = C_L \frac{\delta V}{\delta t}$$

This current flows in the inductance $L_G$, and causes a voltage drop

$$V_G = L_G \frac{\delta i}{\delta t}$$

which appears directly on the ground pin of the driver, as in figure 3.7.

Fig 3.7 Ground bounce caused by discharge of the output capacitor.

The voltage drop on the ground lead appears directly at the outputs in the LOW state, since these are connected to ground through the driver output transistor. The HIGH outputs are connected to the power supply $V_{CC}$ and get only second order effects (due to the current spike through the totem-pole output and parasitic coupling).

Fig 3.8 Effects of ground bounce on steady outputs.

The same model can be applied for LOW-HIGH transitions, taking into account parasitic inductance of supply interconnections. Now the voltage drop appears directly at the outputs in the HIGH state, connected to $V_{CC}$; LOW outputs get only second order effects (figure 3.9).
The induced noise is proportional to the current spike, and this in turn is higher when several outputs change state at the same time, this disturbance is therefore called **simultaneous switching noise**.

### Numerical example 2

An Integrated Circuit contains 8 drivers, in a DIP 20 package. Each driver works in the conditions of example 1 (a current peak of 300 mA when the output changes logic state). The total peak current is

$$8 \times 0.3 = 2.4 \text{ A}$$

Assuming a triangular current waveform with total duration 4 ns (the voltage rise time), and peak value 4.8 A (doubled, to keep the same area, which corresponds to the same total charge moved in/out the capacitor), the slew rate of the current is:

$$\frac{\Delta I}{\Delta t} = \frac{4.8 \text{ A}}{2 \text{ ns}} = 2.4 \text{ A/ns}$$

With 10 nH inductance for the ground pin (optimistic assumption, since the 20 pin DIL is slightly larger than the 14-pin), the amplitude of the ground bounce is

$$V = L \frac{\Delta I}{\Delta t} = 10 \text{ nH} \times 2.4 \text{ A/ns} = 2.4 \text{ V}$$

Since the input signals $V_I$ are referred to system ground, the same voltage drop $V_G$ appear at the input of drivers, and changes $V_I$ to $V'_I = V_I - V_G$. Therefore the drop on ground lead caused by output current spikes may also induce false logic states at the inputs.
Review questions

1) Simultaneous switching noise caused by low-to-high state change affects
   - mostly the outputs at low logic state,
   - mostly the outputs at high logic state,
   - only the outputs at low logic state,
   - the outputs at low and at high logic state in equal way.

   In L > H transitions the output capacitance is charged from the power supply. The current flowing in the supply pin may shift the actual supply voltage of the device, thus changing the HIGH output level.

2) Simultaneous switching noise caused by high-to-low state change affects
   - mostly the outputs at low logic state,
   - mostly the outputs at high logic state,
   - only the outputs at high logic state,
   - the outputs at low and at high logic state in equal way.

   In H > L transitions the output capacitance is discharged towards GND. The current flowing in the ground pin may shift the actual ground of the device, thus changing the LOW output level.

3) Increasing the capacitive load
   - increases the ground bounce mostly in H>L output transitions,
   - increases the ground bounce only in L>H output transitions,
   - increases the ground bounce both in H>L and in L>H output transitions,
   - does not modify the ground bounce.

   Increasing the output capacitance increases the amount of charges to be removed to shift the output voltage from $V_{OH}$ to $V_{OL}$. These charges make the current flowing in the ground pin, which may shift the actual ground of the device, thus causing the ground bounce.

4) Increasing the resistance of common ground connections may cause ground bounce because of
   - totem pole current spike,
   - charge current in L>H output transitions,
   - discharge current in H>L output transitions,
   - steady-state currents in the IC.

   In H > L transitions the output capacitance is discharged towards GND. The discharge current flows in the ground pin, and causes a shift of the actual ground of the device.

5) 16 outputs with a capacitive load of 100 pF each switch together from 5V to 0V; the fall time is 5 ns; the ground connection has a 1 ohm equivalent resistance. The expected ground bounce is:
   - 0.8 V, 1.6 V, 3.2 V, 4.8 V.

   The slew rate $dv/dt$ is 1V/ns; the current can be evaluated as $I = C/(dv/dt)$. The total capacitance is 100 pF x 16 = 1.6 nF. Since $V = R x I$:

   \[
   \text{Ground bounce } V = 1 \text{ ohm} \times \left(1.6 \text{ nF} / (1 \text{ V/ns})\right) = 1.6 \text{ V}
   \]

Signal Integrity in Digital Circuits

Lesson 4: Design guide for ground and power distribution

Summary

Currents must flow in digital circuits to power the active devices and charge/discharge parasitic capacitance; these same currents flow in ground and supply conductors and may cause false signaling because of ground bounce and simultaneous switching noise. This lesson presents the techniques to distribute ground and supply to ICs in such a way as to minimize this kind of noise. Reducing the disturbance of an electronic system towards itself reduces also the Electro Magnetic Interference (EMI) radiated to the external world.

This lesson answers to the following questions:

- How can the designer predict the amount of ground bounce?
- Which logic family must be chosen to minimize switching noise?
- Which is the influence of board layout on switching noise?
- How can bypass capacitors reduce ground bounce and switching noise?
- Which are the best techniques to distribute ground and power supplies in high speed digital circuits?
- How should we distribute clock signals?

References

For this lesson, the related sections in the reference book are: 5.2, 5.3, 5.4, 5.8, 7.4, 8.4, 11.2, and 11.5.

Decoupling Capacitors

To reduce the effects of ground bounce and simultaneous switching the designer should take several steps, some similar to the ones which reduce crosstalk:

- use slow logic circuits;
- minimize capacitive loads;
- reduce impedance of ground and supply connections;
- insert bypass capacitors between supply and ground.

The peak output current depends on capacitive load, that is on the number of inputs connected to the driver. In the case of bus lines, a transceiver insulates the bus line from internal board loads, thus reducing ground bounce in bus drivers.
The model to show the effect of bypass capacitors is in figure 4.1. Two devices receive ground and power supply from partially common conductors. When the output stage of the driver requires some current, it must come from the power supply through the power and ground connection, which have some equivalent resistance and inductance (only the inductance is shown in the equivalent circuit). These current causes voltage drops: the ground bounce and the switching noise.

The voltage drop on the wire inductance caused by current of device 1 affects also the device 2.

![Fig 4.1. Current path with no bypass capacitor](image1)

The bypass capacitor act as local storage for electrical charges to be used for current pulses caused by Totem Pole output switch and charge/discharge of parasitic output capacitance. With a bypass capacitor the current flow and voltage drops are modified as in figure 4.2. The voltage drop caused by the current of device 1 does not affect the supply voltage of device 2 (V2). In this scheme however, these drop still affect the power supply of device 1.

![Fig 4.2. Current path with a bypass capacitor](image2)

A better positioning is shown in figure 4.3: connecting the capacitor directly to the ground and supply pin of the device minimizes all voltage drops causes by current flowing in ground or supply conductors (as long as we do not consider the inductance of the capacitor itself – see later)

![Fig. 4.3 Bypass capacitor directly on device supply pin: the voltage V2 is not affected by currents of device 1.](image3)

The bypass capacitor can be placed also in other positions, provided that the current required by device 1 could be supplied without causing voltage drops on the ground/supply connections of device 2. Figure 4.4 is an example of incorrect positioning.

![Fig 4.4 Incorrect placements of the bypass capacitor: V2 is affected by drops on L2 and L5.](image4)
Even with bypass capacitors, the impedance of ground and power supply conductor must be kept as low as possible. Reducing this impedance reduces the voltage drop for a given current. To reduce inductance, resistance, and impedance use wide tracks, or continuous ground/supply planes.

The impedance of all conductors in the ground-supply path must be low, and this includes the bypass capacitor itself. The impedance of a capacitor should decrease with frequency, but real components have series inductive and resistive components, caused by leads and dielectric losses (figure 4.5).

![Fig. 4.5 A real capacitor](image)

The impedance diagram for the real capacitor (figure 4.6) has a capacitive zone (left – for low frequency the inductance can be considered a short circuit), and an inductive zone (right – for high frequency the capacitor can be considered a short circuit), where impedance goes up with the frequency. Between these two, we can define a resonant frequency, where the impedance is reduced to a minimum value (only resistive loss).

![Fig. 4.6 Impedance of ideal (blue) and real capacitor (red).](image)

The parasitic inductance depends mainly from the package; capacitors of different values but with the same package have different impedance in the capacitive zone, but almost identical behavior in the inductive zone. Capacitors with the same nominal value but different package or different type have identical behavior in the capacitive zone, and different impedance for high frequency, as shown in figure 4.7a and 4.7b.

![Fig 4.7 a) Different capacitance value in the same package](image)

The best bypass capacitors to be placed close to switching devices are multilayer ceramic, shown in figure 4.8 (leaded packages) and 4.9 (surface mount).

![Fig 4.8 Multilayer ceramic bypass capacitors in leaded packages (each division on the top is 1 mm)](image)

![Fig 4.9 Multilayer ceramic bypass capacitors in surface mount package (compare the size; here too each division on the top is 1 mm).](image)
A first rough rule for effective bypass is to use one multilayer ceramic 10-100 nF, placed close to the IC (about one capacitor every 10 drivers). Capacitor leads add inductance, and must be kept as short as possible; surface mount devices, with direct connection to supply and ground conductors are better than Pin Through Hole (PTH) devices.

The minimum value for a bypass capacitors can be evaluated from the circuit in figure 4.10.

\[
\Delta V_{Cs} = \Delta V_{CL} \cdot \frac{C_L}{C_s}
\]

For instance, if 16 outputs with 30 pF capacitive load switch together from 0 V to 5 V, and if the desired change in supply voltage is 0.1 V:

\[
C_s = \frac{5V \times (16 \times 30 \text{ pF})}{0.1 \text{ V}} = 24 \text{ nF}
\]

Higher values can be used, as long as this does not increase the parasitic inductance. Consider that large capacitors (e.g. aluminium electrolytic) have good behavior at low frequency, but the wide case causes large inductive components. To achieve low impedance over a wide range of frequency we must put in parallel capacitors of different values and types. Small ones will be placed as close as possible to the switching devices, to supply the charges through low-inductance wires (typically one capacitor per small package). Large ones are placed on arrays of packages, or at board level.

Placement of bypass capacitors

Bypass capacitors store charges close the places where these are needed (the driver IC supply and ground pins), and provide the peak current through low-impedance paths.

The printed circuit boards must be designed for a short distance between power and ground. This is done by using power and ground planes, which can be electrically approximated with distributed capacitance. A bypass capacitor as close as possible to the power and GND pins of the device helps to provide a low-impedance path for the transient currents.

Numerical example

Consider a device driving a line from L to H having an impedance (Z @ 100 Ω) and a supply voltage (Vcc = 5 V). The current needed to shift the line voltage is 50 mA. For eight outputs switching the total current is I = 50 × 8 = 400 mA. The current is provided by the power line (or plane) in a period which can be estimated as 3 times the rise time of the output (for instance approximately 3 ns for ABT). The bypass capacitor must supply the charge in that same period of time to avoid Vcc drop, therefore supply connection inductance becomes an important issue. The inductance is directly proportional to the distance between the lines as well as the length of the lines. By reducing the loops, we can minimize the inductance and allow the capacitor to do its function more efficiently, and hence keep the noise off the power line (or plane).

A more complete document on bypass capacitors is available from http://www.ti.com/sc/docs/psheets/appnote.htm

Ground and power distribution

The most effective technique to keep low inductance in ground and power distribution is to use continuous planes; this is not possible for single layer or double-layer PCB, where ground/power distribution must compete with signal tracks. Suitable distribution schemes are in the following figures. For each scheme the blue arrow (middle diagram) shows the ground-supply loop, that is the path of currents during the Totem Pole switching, and the orange arrow (right diagram) shows the path of the return current for the signal track shown (black line).

The finger layout in figure 4.12 uses only one layer, but forces the supply current and the signal return current to flow in wide-area loops.
Rearranging the fingers as in figure 4.13 cuts the supply current loop area, but keeps a wide signal-return loop (and uses two different layers).

The grid scheme in figure 4.14 requires bypass capacitors on each device to reduce loop area both for supply and return currents (at each crossing a bypass capacitor provides a path for fast-changing currents).

Clock distribution

Distribution of clock signals is a critical issue in high speed logic systems. The clock synchronizes the operations, and state changes of logic signals are related with clock edge time position. To comply with timing specification of sequential logic circuits, the clock must reach each part of the system at the same time, that is with limited skew $t_K$ (the skew reduces the set-up and hold time margins).

Multidrop connections (figure 4.16) introduce skew because of different positions of receivers along the line.
The star connection, with series termination on each line at driver side, as in figure 4.17, it is possible allows the designer to insert equal delays between the driver and each clocked device. Each interconnection must have the same parameters and length; this equalizes the transmission delays. Several lines conger to the same point (the driver output), and it is difficult to get line impedance matching.

Fig. 4.17 Star distribution from a single driver.

An even better solution is to drive each line with a separate buffer, as in figure 4.18. Specific devices, with matched-delay buffers are available for this task. With \( R_S = Z_0 - R_O \) the interconnection lines are matched at the near end, no reflection occurs on the driver, and each signal is fully settled within 2 \( t_P \).

Fig. 4.18 Star distribution with multiple drivers.

For better matching of propagation times, line length can be equalized by proper PCB layout; the track follows a winding path, to put a consistent electrical length in a narrow space, as in figure 4.19.

Fig. 4.19 Equalization of delays on PCB tracks.

Review questions

1) To reduce ground bounce

- use high current drivers
- reduce capacitive loading of outputs
- use terminated transmission lines
- raise the impedance of ground connections

The ground bounce is caused by the current spike required to (dis)charge the output capacitance. This current increases as the total capacitance at the output of the driver is increased. The termination of transmission lines does not affect the ground bounce, and all other answers bring to an increase of the bounce.

2) An acceptable value for local bypass capacitors is

- 10 pF
- 100 pF
- 100 nF
- 10 F

The bypass capacitor must supply the charges required by the totem-pole current spike, and to charge or discharge to output capacitance. The actual value can change depending on the parameters of the IC and of the interconnection, but a value of 100 nF is correct in most cases. Too small capacitors (less than 1 nF) cannot store enough charges, and too large ones have large size with higher parasitic inductance.

3) The bypass capacitor must be placed

- as close to the power supply as possible
- as close as possible to devices which need high static current
- as close as possible to devices with high dynamic current consumption
- anywhere in the system

The electric charge stored in the bypass capacitor reach the output stage of the driver through the ground and supply connections. The voltage drop is proportional to the resistance and inductance of these connections. Placing the capacitor as close as possible to the IC reduces resistance and inductance on the current paths.

4) The preferred device as a bypass capacitor for high speed digital circuit is:

- aluminium electrolytic capacitor
- multilayer ceramic, axial lead
- multilayer ceramic, radial lead
- multilayer ceramic, surface mount

The bypass capacitor must have a capacitive behavior in the frequency range corresponding to the harmonic content of driver current spikes. With 2 ns rise-fall times the significant power of the harmonics is around 50 MHz and above. The best capacitors are SMD, due to very short and low-impedance connections towards the supply and ground plane.

5) A smaller package helps to reduce ground bounce because:

- has better heat dissipation,
- has less inductance on GND conductors
- has less capacitance among adjacent pins
- has thinner wires towards ground.

Smaller packages have shorter \( V_{OC} \) and GND connections – and therefore less parasitic inductance - from the silicon die to the IC pin.
6) Il a capacitor is modeled as a LRC serial circuit, the minimum value of impedance is for a frequency $F$:

$$F = \frac{1}{LC} \quad F = \frac{1}{\sqrt{L \cdot C}}$$
$$F = \frac{R}{\sqrt{L \cdot C}} \quad F = \sqrt{LC}$$

The impedance of an inductance $L$ is $Z_L = j\omega L$, and the impedance of a capacitor $C$ is $Z_C = 1/j\omega C$. The total impedance is:

$$Z = j\omega L + \frac{1}{j\omega C} = \frac{-\omega^2 LC + 1}{j\omega C}$$

For $\omega^2 = 1/LC$, $Z = 0$.

7) For frequency above resonance, a capacitor behaves as:

- pure inductance
- pure resistance
- parallel LC
- series R and L

With a R L C series model, above the resonant frequency the capacitive impedance is far less than the inductive and resistive terms. The capacitor can be modeled as a R-L serial circuit.